HEWLETT PACKARD

High Speed Optocouplers

Technical Data

6N135
6N136
HCPL-2502
HCPL-4502
HCPL-4503

Features

- **Very High Common Mode Transient Immunity: 15000 V/μs at V_{CM} = 1500 V Guaranteed (HCPL-4503)**
- **High Speed: 1 Mb/s**
- **TTL Compatible**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **Open Collector Output**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 Vac, 1 Minute and 5000 Vac, 1 Minute (Option 020).**
- **VDE 0883 Approval Pending**

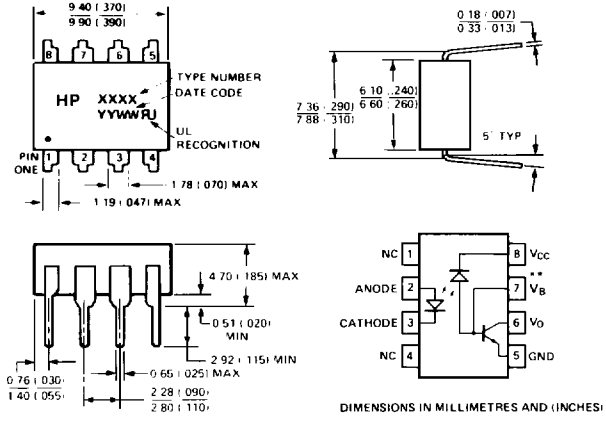
Description

These diode-transistor optocouplers use an insulating layer between the light emitting diode and an integrated photon detector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output transistor collector increase the speed up to a hundred times over that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

Outline Drawing



*See notes, following page.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired such as in the feedback path of switch-mode power supplies. CTR is 15 to 22% at I_F = 16mA.

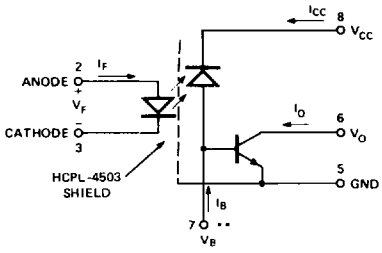
The HCPL-4502 provides the electrical and switching performance of the 6N136 with increased ESD protection.

The HCPL-4503 is an HCPL-4502 with increased common mode transient immunity of 15000 V/μs minimum at V_{CM} = 1500 guaranteed.

Applications

- **Video Signal Isolation**
- **Line Receivers** – High common mode transient immunity (>1000 V/μs) and low input-output capacitance (0.6 pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5 V to 30 V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Schematic



**NOTE: FOR HCPL-4502/3, PIN 7 IS NOT CONNECTED

Absolute Maximum Ratings

Storage Temperature * ..... -55°C to +125°C
Operating Temperature* ..... -55°C to 100°C
Lead Solder Temperature* ..... 260°C for 10s
(1.6 mm below seating plane)
Average Input Current – I_F* ..... 25 mA[1]
Peak Input Current – I_F* ..... 50 mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F* ..... 1.0 A
(≤1 μs pulse width, 300 pps)
Reverse Input Voltage – V_R* (Pin 3-2) ..... 5 V
Input Power Dissipation* ..... 45 mW[3]
Average Output Current – I_O* (Pin 6) ..... 8 mA
Peak Output Current* ..... 16 mA
Emitter-Base Reverse Voltage * ..... 5 V
(Pin 5-7, except HCPL-4502/3)
Output Voltage* – V_O (Pin 6-5) ..... -0.5 V to 15 V
Supply Voltage* – V_{CC} (Pin 8-5) ..... -0.5 V to 15 V
Output Voltage – V_O (Pin 6-5) ..... -0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5) ..... -0.5 V to 30 V
Base Current – I_B* (Pin 7, except HCPL-4502/3) ..... 5 mA
Output Power Dissipation* ..... 100 mW[4]

*JEDEC Registered Data (The HCPL-2502 and HCPL-4502/3 are not registered.)

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 13.

Parameter	Symbol	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18	50	%	T_A = 25°C, V_O = 0.4 V; I_F = 16 mA, V_{CC} = 4.5 V	1, 2 4	5, 11
			5	19			V_O = 0.5 V		
		6N136 HCPL-4502 HCPL-4503	19	24	50	%	T_A = 25°C, V_O = 0.4 V		
			15	25			V_O = 0.5 V		
		HCPL-2502	15	18	22	%	T_A = 25°C, V_O = 0.4 V		
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA; I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA		
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA		
					0.5		I_O = 2.4 mA		
Logic High Output Current	I_{OH}*			0.003	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V; I_F = 0 mA	6	
				0.01	1		T_A = 25°C, V_O = V_{CC} = 15.0 V		
					50				
Logic Low Supply Current	I_{CCL}			50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		13
Logic High Supply Current	I_{CCH}*			0.02	1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		13
					2				
Input Forward Voltage	V_F*			1.5	1.7	V	T_A = 25°C, I_F = 16 mA	3	
					1.8				
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		2500			V_{RMS}	RH < 50%, t = 1 min., T_A = 25°C		6
		OPT. 020	5000			V_{RMS}			
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		6
Transistor DC Current Gain	h_{FE}			150			V_O = 5 V, I_O = 3 mA		
				130			V_O = 0.4 V, Ib = 20 µA		

*For JEDEC registered parts. **All typicals at T_A = 25°C.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}*	6N135		0.2	1.5	μs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.2	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Propagation Delay Time to Logic High at Output	t_{PLH}*	6N135		1.3	1.5	μs	T_A = 25°C, R_L = 4.1 kΩ	5, 9, 11	8, 9
					2.0				
		6N136 HCPL-2502 HCPL-4502 HCPL-4503		0.6	0.8		T_A = 25°C, R_L = 1.9 kΩ		
					1.0				
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	6N135		1		kV/μs	R_L = 4.1 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 0 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	6N135		1		kV/μs	R_L = 4.1 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V_{p-p}	10	7, 8, 9
		6N136 HCPL-2502 HCPL-4502		1			R_L = 1.9 kΩ		
		HCPL-4503	15	30			R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C, V_{CM} = 1500 V_{p-p}		
Bandwidth	BW			9		MHz	See Test Circuit	7, 8	10

*For JEDEC registered parts.
**All typicals at T_A = 25°C.

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
8. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
9. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below its mid-frequency value.
11. The JEDEC registration for the 6N136 specifies a minimum CTR of 15%. HP guarantees a minimum CTR of 19%.
12. See Option 020 data sheet for more information.
13. Use of a 0.1 μf bypass capacitor connected between pins 5 and 8 is recommended.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(I01)	≥ 7	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(I02)	≥ 7	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Insulation thickness between emitter and detector
Tracking Resistance	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group (Per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

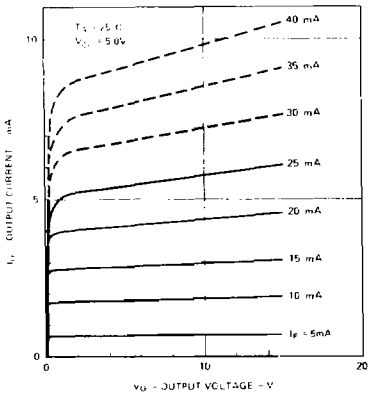


Figure 1. DC and Pulsed Transfer Characteristics.

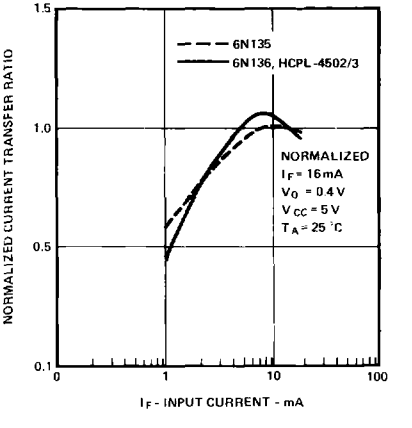


Figure 2. Current Transfer Ratio vs. Input Current.

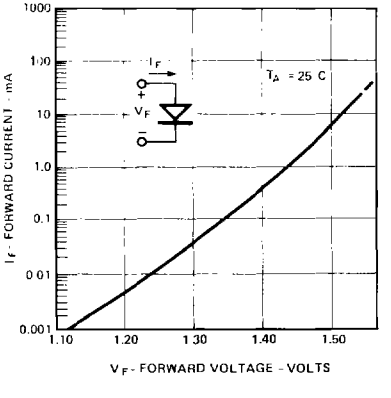


Figure 3. Input Current vs. Forward Voltage.

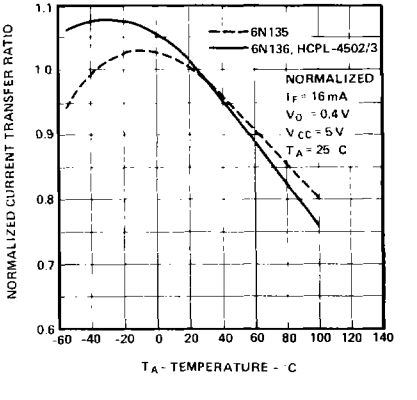


Figure 4. Current Transfer Ratio vs. Temperature.

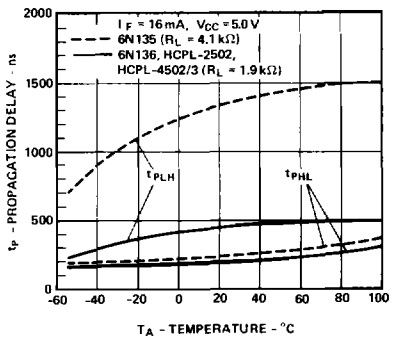


Figure 5. Propagation Delay vs. Temperature.

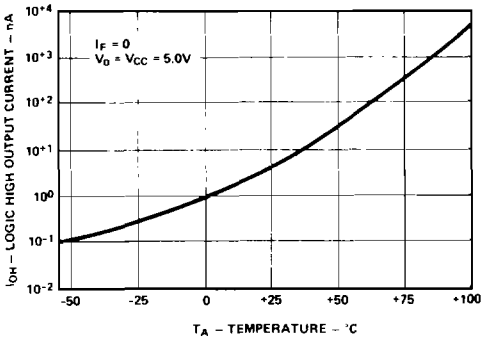


Figure 6. Logic High Output Current vs. Temperature.

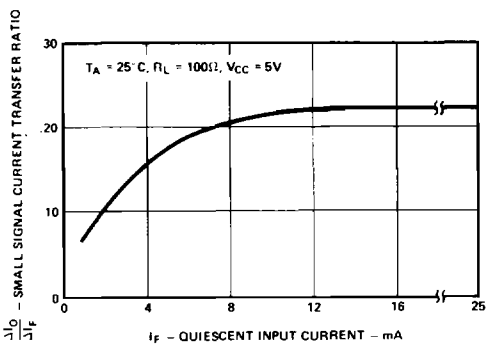


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

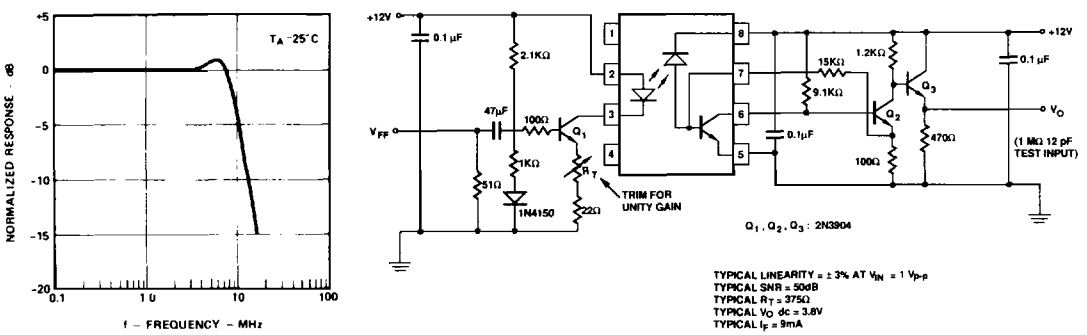


Figure 8. Frequency Response.

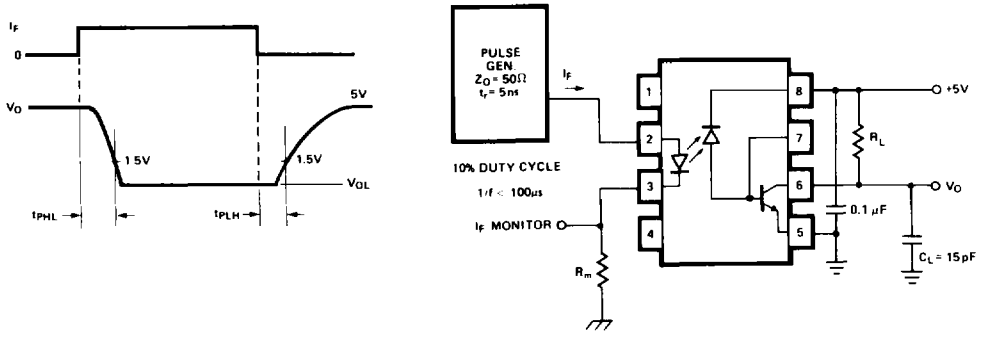


Figure 9. Switching Test Circuit.*

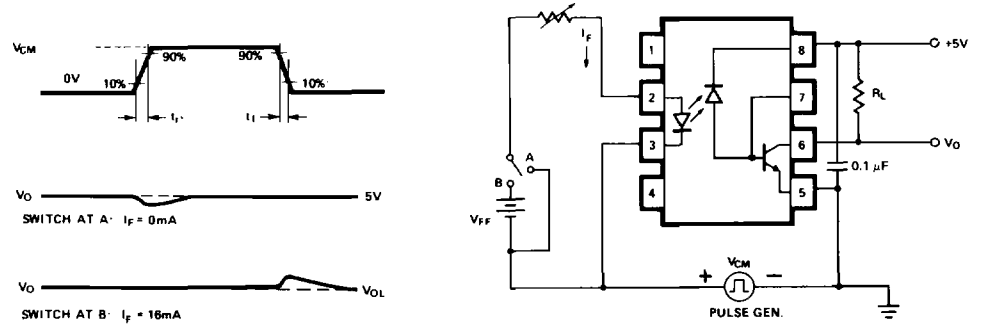


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

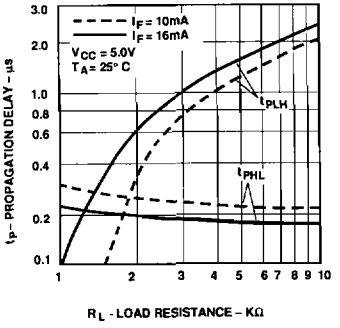


Figure 11. Propagation Delay Time vs. Load Resistance.

*JEDEC Registered Data