FUJITSU

# CMOS UV ERASABLE 131072-BIT READ ONLY MEMORY

**MBM 27C128-17**
**MBM 27C128-20**
**MBM 27C128-25**

February 1987
Edition 2.0

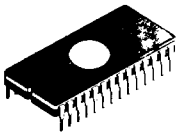
## CMOS 131072 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C128 is a high speed 131,072 bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

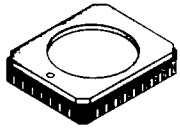
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C128 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- CMOS power consumption
  Standby : 100μA max.
  Active : 30mA max.
- 16,384 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulses
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time :
  170ns max. (MBM 27C128-17)
  200ns max. (MBM 27C128-20)
  250ns max. (MBM 27C128-25)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ± 10% tolerance
- Standard 28-pin Ceramic DIP : (Suffix: -Z)
- Standard 32-pad Ceramic LCC : (Suffix: -TV)

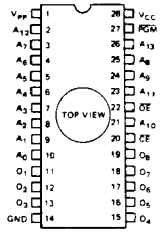


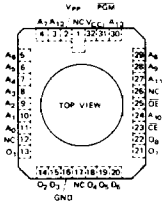
CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-F01

**PIN ASSIGNMENT**




**ABSOLUTE MAXIMUM RATINGS (See NOTE)**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Temperature under Bias | $T_{BIAS}$ | -25 to +85 | °C |
| Storage Temperature | $T_{STG}$ | -65 to +125 | °C |
| All Inputs/Outputs Voltage with Respect to GND | $V_{IN}$, $V_{OUT}$ | -0.6 to $V_{CC}$+0.6 | V |
| Voltage on $A_9$ with Respect to GND | $V_{A9}$ | -0.6 to +13.5 | V |
| $V_{PP}$ Voltage with Respect to GND | $V_{PP}$ | -0.6 to +22 | V |
| Supply Voltage with Respect to GND | $V_{CC}$ | -0.6 to +7 | V |

**NOTE:** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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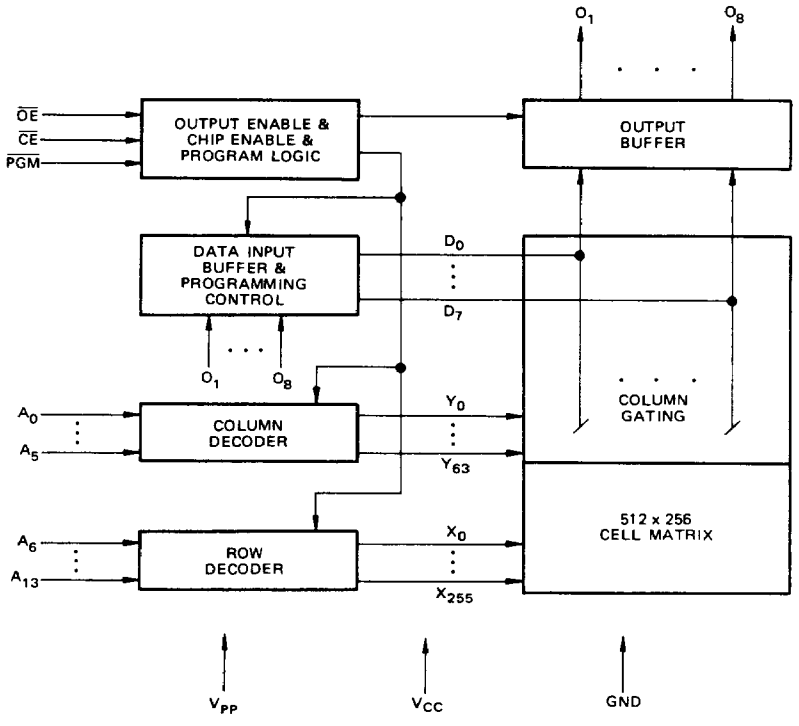
Fig. 1 – MBM 27C128 BLOCK DIAGRAM




## CAPACITANCE ($T_A$ = 25°C, f = 1MHz)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Input Capacitance ($V_{IN}$ = 0V) | $C_{IN}$ | | 4 | 6 | pF |
| Output Capacitance ($V_{OUT}$ = 0V) | $C_{OUT}$ | | 8 | 12 | pF |

## FUNCTIONS AND PIN CONNECTIONS

| Mode \ Function (Pin No.) | Address Input (2 to 10, 21, 23 to 26) | Data I/O (11~13, 15~19) | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $V_{CC}$ (28) | $V_{PP}$ (1) | GND (14) |
|---|---|---|---|---|---|---|---|---|
| Read | $A_{IN}$ | $D_{OUT}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | GND |
| Output Disable | $A_{IN}$ | High-Z | $V_{IL}$ | $V_{IH}$ | Don't Care | $V_{CC}$ | $V_{CC}$ | GND |
| | | | | Don't Care | $V_{IL}$ | | | |
| Standby | Don't Care | High-Z | $V_{IH}$ | Don't Care | Don't Care | $V_{CC}$ | $V_{CC}$ | GND |
| Program | $A_{IN}$ | $D_{IN}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{CC}$ | $V_{PP}$ | GND |
| Program Verify | $A_{IN}$ | $D_{OUT}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | $V_{PP}$ | GND |
| Program Inhibit | Don't Care | High-Z | $V_{IH}$ | Don't Care | Don't Care | $V_{CC}$ | $V_{PP}$ | GND |

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## RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{CC}$ Supply Voltage*1 | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| $V_{PP}$ Supply Voltage | $V_{PP}$ | $V_{CC}$-0.6 | | $V_{CC}$+0.6 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | | $V_{CC}$+0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.1 | | 0.8 | V |
| Operating Temperature | $T_A$ | 0 | | 70 | °C |

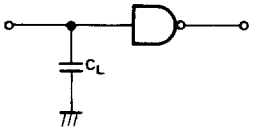
**Note:** *1 $V_{CC}$ must be applied either before or coincident with $V_{PP}$ and removed either after or coincident with $V_{PP}$.

## DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Input Load Current ($V_{IN}$ = 5.5V) | $\|I_{LI}\|$ | | | 10 | μA |
| Output Leakage Current ($V_{OUT}$ = 5.5V) | $\|I_{LO}\|$ | | | 10 | μA |
| $V_{PP}$ Supply Current | $I_{PP1}$ | | 1 | 100 | μA |
| $V_{CC}$ Standby Current ($\overline{CE}$ = $V_{IH}$) | $I_{SB1}$ | | | 1 | mA |
| $V_{CC}$ Standby Current ($\overline{CE}$ = $V_{CC}$±0.3V, $I_{OUT}$ = 0mA) | $I_{SB2}$ | | 1 | 100 | μA |
| $V_{CC}$ Active Current ($\overline{CE}$ = $V_{IL}$, $I_{OUT}$ = 0mA) | $I_{CC1}$ | | 2 | 30 | mA |
| $V_{CC}$ Operation Current (f = 4MHz, $I_{OUT}$ = 0mA) | $I_{CC2}$ | | 4 | 30 | mA |
| Output Low Voltage ($I_{OL}$ = 2.1mA) | $V_{OL}$ | | | 0.45 | V |
| Output High Voltage ($I_{OH}$ = -400μA) | $V_{OH1}$ | 2.4 | | | V |
| Output High Voltage ($I_{OH}$ = -100μA) | $V_{OH2}$ | $V_{CC}$-0.7 | | | V |

**Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGRAMMING)**

| | |
|---|---|
| Input Pulse Levels: | 0.8V to 2.2V |
| Input Rise and Fall Times: | ≤ 20ns |
| Timing Measurement Reference Levels: | 1.0V and 2.0V for inputs<br>0.8V and 2.0V for outpust |
| Output Load: | 1 TTL gate and $C_L$ = 100pF |

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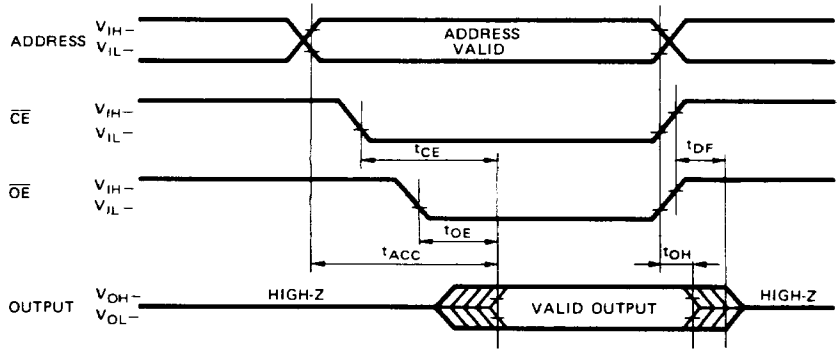
# AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted)**

| Parameter | Symbol | MBM 27C128-17 | | | MBM 27C128-20 | | | MBM 27C128-25 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Address Access Time*1 | $t_{ACC}$ | | | 170 | | | 200 | | | 250 | ns |
| $\overline{CE}$ to Output Delay | $t_{CE}$ | | | 170 | | | 200 | | | 250 | ns |
| $\overline{OE}$ to Output Delay*1 | $t_{OE}$ | | | 70 | | | 70 | | | 100 | ns |
| Address to Output Hold | $t_{OH}$ | 0 | | | 0 | | | 0 | | | ns |
| Output Enable High to Output Float*2 | $t_{DF}$ | 0 | | 60 | 0 | | 60 | 0 | | 60 | ns |

**Notes:** *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
*2 $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

**OPERATION TIMING DIAGRAM**



# PROGRAMMING/ERASING INFORMATION

## PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C128 has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM 27C128 through the procedure of programming.

### Standard Programming

The programming mode is entered when +21V is applied to the $V_{PP}$ pin and $\overline{CE}$ and $\overline{PGM}$ are both at $V_{IL}$. During programming, $\overline{CE}$ is kept at $V_{IL}$. A 0.1$\mu$F capacitor between $V_{PP}$ and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. the procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

### Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 27C128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm utilizes a sequence of a 1ms pulse to program each location. The programming mode is entered when +21V and +6V are applied to the $V_{PP}$ pin and $V_{CC}$ pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are $V_{IH}$. During programming, $\overline{CE}$ is kept at $V_{IL}$. A 0.1$\mu$F capacitor between $V_{PP}$ and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit patgterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (Address=G)
2) Set the $V_{CC}$=6V and $V_{PP}$=21V
3) Input data.
4) Compare the input data with FF. If data are FF, go to the step 11). If not, proceed the next step.
5) Clear the counter (X←0).
6) Apply ONE programming pulse to $\overline{PGM}$ pin ($t_{PW}$ = 1ms Typ.).
7) Inclement the counter (X←X+1).
8) Compare the counter value with 20. If X=20, go to the step 10). If X<20, proceed the next step.
9) Verify the data. If the programmed data are the same as the input data, proceed the next step. If not, go back to the step 6).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1ms x X or Xms x 1).
11) Compare the address with the end address. If the programmed address is the end address, proceed the next step. If not, go back to the step 3) for next address (G←G+1).
12) Verify the data. If the programmed data are not the same as the input data, the part is failed. If the programmed data the same as the input data, programming is at an end.

All that is required is that initial 1 msec program pulse and additional program pulse (21 msec Max.) be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 21 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

## ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C128 to an ultraviolet light source. A dosage of 15 W-seconds/cm$^2$ is required to completely erase an MBM 27C128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000$\mu$W/cm$^2$ for 15 to 21 minutes. The MBM 27C128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C128 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although

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# PROGRAMMING/ERASING INFORMATION (continued)

erasure time will be much longer than with an UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C128, and exposure to the device should be prevented to realize maximum system reliability. If used in light environment, the package windows should be covered by an opaque label or substance.

## ELECTRONIC SIGNATURE

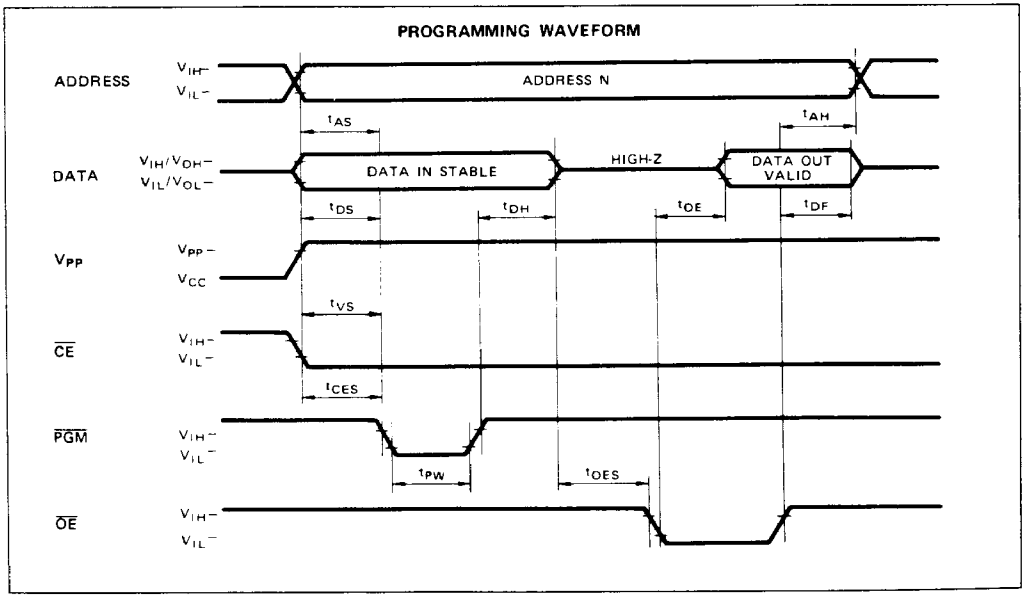
The MBM 27C128 has an electronic signature mode which can be intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to the address line $A_9$ (pin 24) of the MBM 27C128. Two identifier bytes are readed out from the outputs by toggling address line $A_0$ (pin 10) from $V_{IL}$ to $V_{IH}$. The address lines from $A_1$ through $A_{13}$ must be hold at $V_{IL}$ during the electronic signature mode. See the table below.

| $A_0$ | $O_1$ | $O_2$ | $O_3$ | $O_4$ | $O_5$ | $O_6$ | $O_7$ | $O_8$ | Definition |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Mnufacture |
| $V_{IH}$ | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | Device |

**Note:** $A_9 = 12V \pm 0.5V$

$A_1$ thru $A_8 = A_{10}$ thru $A_{13} = \overline{CE} = \overline{OE} = V_{IL}$.



## 1. Standard Programming

### DC CHARACTERISTICS

($T_A$ = 25±5°C, $V_{CC}$*1 = 5V±5%, $V_{PP}$*2 = 21±0.5V)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Input Leakage Current ($V_{IN}$ = 5.25V/0.45V) | $I_{LI}$ | | | 10 | μA |
| $V_{PP}$ Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = $V_{IL}$) | $I_{PP2}$ | | | 40 | mA |
| $V_{CC}$ Supply Current | $I_{CC3}$ | | | 30 | mA |
| Input Low Level | $V_{IL}$ | -0.1 | | 0.8 | V |
| Input High Level | $V_{IH}$ | 2.0 | | $V_{CC}$+0.3 | V |
| Output Low Voltage During Verify ($I_{OL}$ = 2.1mA) | $V_{OL}$ | | | 0.45 | V |
| Output High Voltage During Verify ($I_{OH}$ = -400μA) | $V_{OH}$ | 2.4 | | | V |

**Note:** *1 $V_{CC}$ must be applied either coincidently or before $V_{PP}$ and removed either coincidently or after $V_{PP}$.
*2 $V_{PP}$ must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining $V_{PP}$ = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = $V_{IL}$, $V_{PP}$ must not be switched from 5 to 21 volts or vise-versa.

### AC CHARACTERISTICS

($T_A$ = 25±5°C, $V_{CC}$ = 5V±5%, $V_{PP}$ = 21±0.5V)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Address Setup Time | $t_{AS}$ | 2 | | | μs |
| Chip Enable Setup Time | $t_{CES}$ | 2 | | | μs |
| Output Enable Setup Time | $t_{OES}$ | 2 | | | μs |
| Data Setup Time | $t_{DS}$ | 2 | | | μs |
| $V_{PP}$ Setup Time | $t_{VS}$ | 2 | | | μs |
| Address Hold Time | $t_{AH}$ | 0 | | | μs |
| Data Hold Time | $t_{DH}$ | 2 | | | μs |
| Output Enable to Output Float Delay | $t_{DF}$ | 0 | | 130 | ns |
| Data Valid from Output Enable | $t_{OE}$ | | | 150 | ns |
| $\overline{PGM}$ Pulse Width | $t_{PW}$ | 25 | 50 | 55 | ms |

# PROGRAMMING/ERASING INFORMATION (continued)

## 2. Quick Programming

### DC CHARACTERISTICS

($T_A$ = 25±5°C, $V_{CC}$*1 = 6V±0.25V, $V_{PP}$*2 = 21V±0.5V)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Input Leakage Current ($V_{IN}$ = 6.25V/0.45V) | $I_{LI}$ | | | 10 | μA |
| $V_{PP}$ Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = $V_{IL}$) | $I_{PP2}$ | | | 40 | mA |
| $V_{CC}$ Supply Current | $I_{CC3}$ | | | 30 | mA |
| Input Low Level | $V_{IL}$ | -0.1 | | 0.8 | V |
| Input High Level | $V_{IH}$ | 2.0 | | $V_{CC}$+0.3 | V |
| Output Low Voltage During Verify ($I_{OL}$ = 2.1mA) | $V_{OL}$ | | | 0.45 | V |
| Output High Voltage During Verify ($I_{OH}$ = -400μA) | $V_{OH}$ | 2.4 | | | V |

**Note:** *1 $V_{CC}$ must be applied either coincidently or before $V_{PP}$ and removed either concidently or after $V_{PP}$.
*2 $V_{PP}$ must not be greater than 22 volts including overshoot. Permanent device damage may occur the device is taken out or put into socket remaining $V_{PP}$ = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = $V_{IL}$, $V_{PP}$ must not be switched from 6 to 21 volts or vise-versa.

### AC CHARACTERISTICS

($T_A$ = 25±5°C, $V_{CC}$ = 6V±0.25V, $V_{PP}$ = 21V±0.5V)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Address Setup Time | $t_{AS}$ | 2 | | | μs |
| Chip Enable Setup Time | $t_{CES}$ | 2 | | | μs |
| Output Enable Setup Time | $t_{OES}$ | 2 | | | μs |
| Data Setup Time | $t_{DS}$ | 2 | | | μs |
| $V_{PP}$ Setup Time | $t_{VS}$ | 2 | | | μs |
| Address Hold Time | $t_{AH}$ | 0 | | | μs |
| Data Hold Time | $t_{DH}$ | 2 | | | μs |
| Output Enable to Output Float Delay | $t_{DF}$ | 0 | | 130 | ns |
| Data Valid from Output Enable | $t_{OE}$ | | | 150 | ns |
| $\overline{PGM}$ Pulse Width | $t_{PW}$ | 0.95 | 1 | 1.05 | ms |

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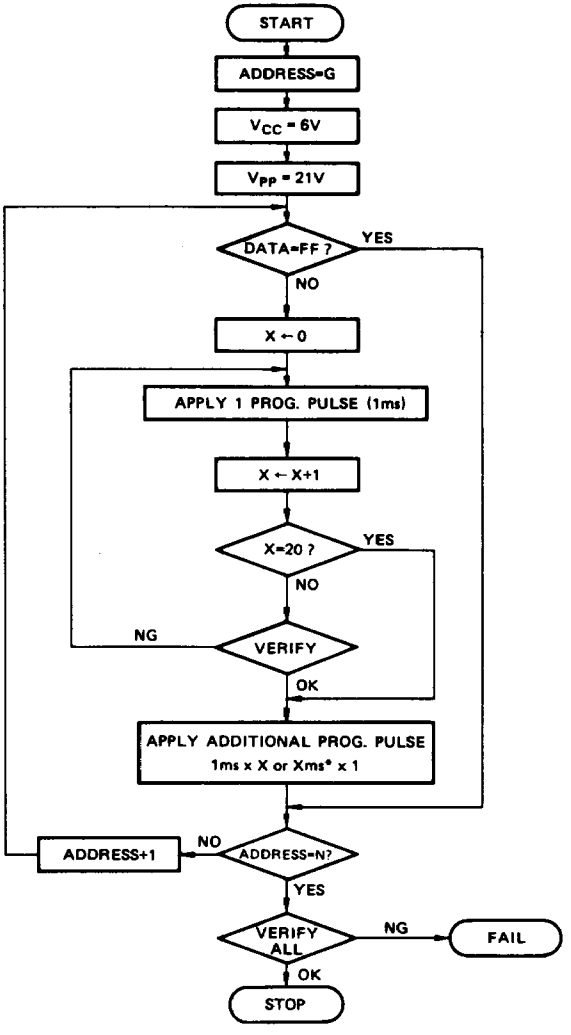
## PROGRAMMING FLOW CHART FOR Quick Pro™

$V_{CC}$ = 6V±0.25V
$V_{PP}$ = 21V±0.5V

$T_{PW}$ = 1ms±50μs
(* = Xms±5%)

G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE

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# PACKAGE DIMENSIONS

**Standard 28-pin Ceramic DIP(Suffix: -Z)**

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)