National Semiconductor

October 20, 2009

ADC10040/ADC10040Q

10-Bit, 40 MSPS, 3V, 55.5 mW A/D Converter

General Description

The ADC10040 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 10-bit digital words at 40 Megasamples per second (MSPS). This converter uses a differential, pipeline architecture with digital error correction and an on-chip sample-and-hold circuit to provide a complete conversion solution, and to minimize power consumption, while providing excellent dynamic performance. A unique sample-and-hold stage yields a full-power bandwidth of 400 MHz. Operating on a single 3.0V power supply, this device consumes just 55.5 mW at 40 MSPS, including the reference current. The Standby feature reduces power consumption to just 13.5 mW.

The differential inputs provide a full scale selectable input swing of 2.0 V_{P-P}, 1.5 V_{P-P}, 1.0 V_{P-P}, with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. An internal +1.2V precision bandgap reference is used to set the ADC full-scale range, and also allows the user to supply a buffered referenced voltage for those applications requiring increased accuracy. The output data format is user choice of offset binary or two's complement.

The ADC10040Q runs on an Automotive Grade Flow and is AEC-Q100 Grade 3 Qualified.

This device is available in the 28-lead TSSOP package and will operate over the industrial temperature range of −40°C to +85°C.

Features

- Single +3.0V operation
- Selectable 2.0 V_{P-P}, 1.5 V_{P-P}, or 1.0 V_{P-P} full-scale input swing
- 400 MHz −3 dB input bandwidth
- Low power consumption
- Standby mode
- On-chip reference and sample-and-hold amplifier
- Offset binary or two's complement data format
- Separate adjustable output driver supply to accommodate 2.5V and 3.3V logic families
- AEC-Q100 Grade 3 Qualified
- 28-pin TSSOP package

Key Specifications

- Resolution .... 10 Bits
- Conversion Rate .... 40 MSPS
- Full Power Bandwidth .... 400 MHz
- DNL .... ±0.3 LSB (typ)
- SNR (f_{IN} = 11 MHz) .... 59.6 dB (typ)
- SFDR (f_{IN} = 11 MHz) .... −80 dB (typ)
- Power Consumption, 40 MHz .... 55.5 mW

Applications

- Ultrasound and Imaging
- Instrumentation
- Cellular Base Stations/Communications Receivers
- Sonar/Radar
- xDSL
- Wireless Local Loops
- Data Acquisition Systems
- DSP Front Ends

Connection Diagram
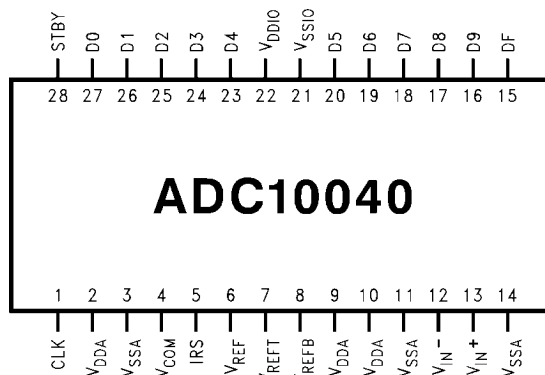
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Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°C)	NS Package	Top Mark	Features
ADC10040CIMT	28 Pin TSSOP	ADC10040CIMT	
ADC10040CIMTX	28 Pin TSSOP Tape & Reel	ADC10040CIMT	
ADC10040QCIMTX	28 Pin TSSOP	ADC10040QCIMT	AEC-Q100 Grade 3 Qualified. Automotive Grade Production Flow
ADC10040QCIMTX	28 Pin TSSOP Tape & Reel	ADC10040QCIMT	AEC-Q100 Grade 3 Qualified. Automotive Grade Production Flow
Use ADC10080EVAL	Evaluation Board	n/a	

Block Diagram
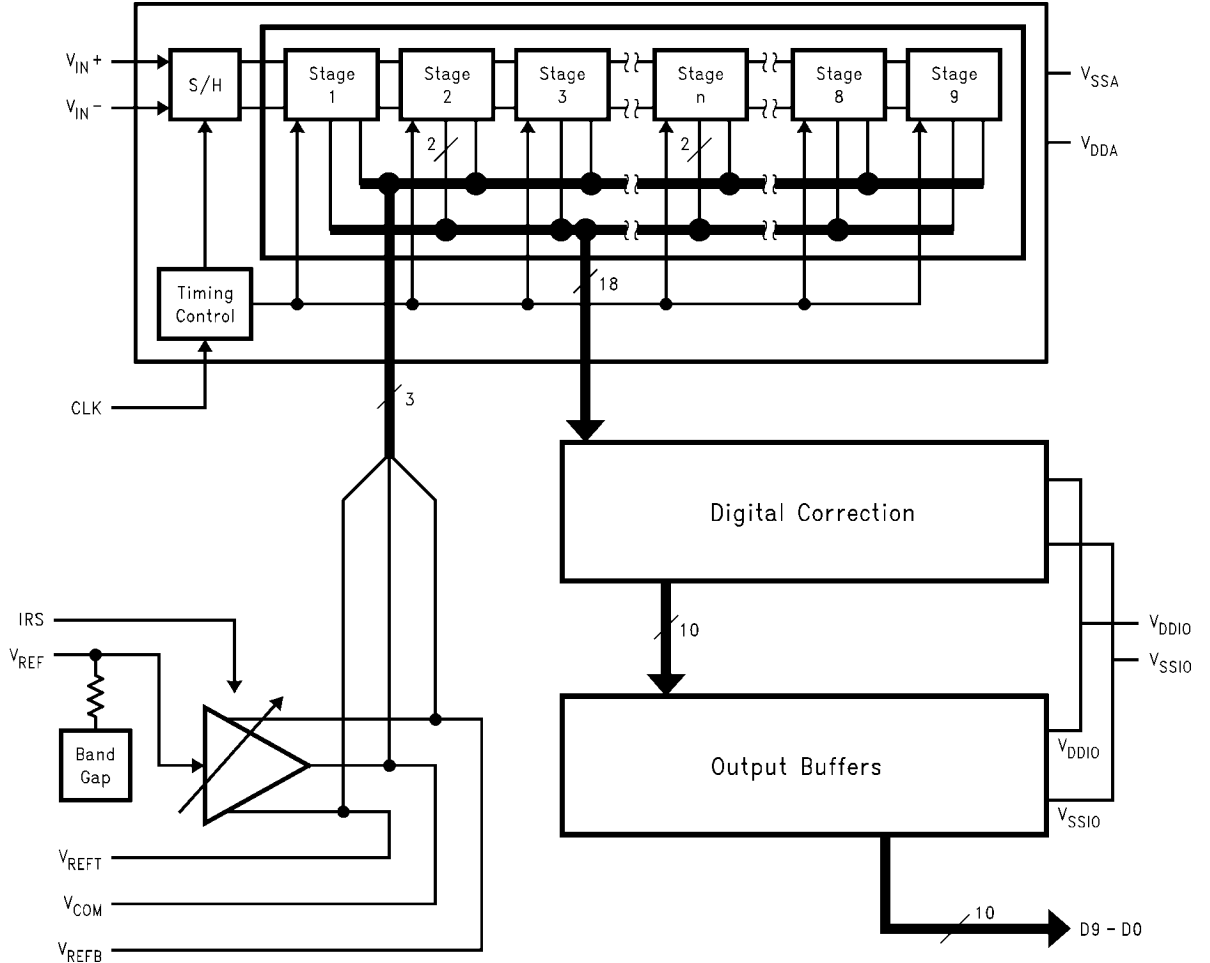
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Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
12	V_{IN-}		Inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 V_{P-P}. This pin may be tied to V_{COM} (pin 4) for single-ended operation.
13	V_{IN+}		Non-inverting analog input signal. With a 1.2V reference the full-scale input signal level is a differential 1.0 V_{P-P}.
6	V_{REF}		Reference Voltage. This device provides an internal 1.2V reference. This pin should be bypassed to V_{SSA} with a 0.1 µF monolithic capacitor. V_{REF} is 1.20V nominal. This pin may be driven by a 1.20V external reference if desired. Do not load this pin.
7 4 8	V_{REFT} V_{COM} V_{REFB}		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to V_{SSA}. These pins should not be loaded. V_{COM} may be used to set the input common mode voltage V_{CM}.
DIGITAL I/O			
1	CLK		Digital clock input. The range of frequencies for this input is 20 MHz to 40 MHz. The input is sampled on the rising edge of this input.
15	DF		DF = "1" Two's Complement DF = "0" Offset Binary
28	STBY		This is the standby pin. When high, this pin sets the converter into standby mode. When this pin is low, the converter is in active mode.
5	IRS (Input Range Select)		IRS = "V_{DDA}" 2.0 V_{P-P} input range IRS = "V_{SSA}" 1.5 V_{P-P} input range IRS = "Floating" 1.0 V_{P-P} input range If using both V_{IN+} and V_{IN-} pins, (or differential mode), then the peak-to-peak voltage refers to the differential voltage (V_{IN+} - V_{IN-}).

Pin No.	Symbol	Equivalent Circuit	Description
16–20, 23–27	D0–D9		Digital output data. D0 is the LSB and D9 is the MSB of the binary output word.

ANALOG POWER

2, 9, 10	V_{DDA}		Positive analog supply pins. These pins should be connected to a quiet 3,0V source and bypassed to analog ground with a 0.1 µF monolithic capacitor located within 1 cm of these pins. A 4.7 µF capacitor should also be used in parallel.
3, 11, 14	V_{SSA}		Ground return for the analog supply.

DIGITAL POWER

22	V_{DDIO}		Positive digital supply pins for the ADC10040's output drivers. This pin should be bypassed to digital ground with a 0.1 µF monolithic capacitor located within 1 cm of this pin. A 4.7 µF capacitor should also be used in parallel. The voltage on this pin should never exceed the voltage on V_{DDA} by more than 300 mV.
21	V_{SSIO}		The ground return for the digital supply for the output drivers. This pin should be connected to the ground plane, but not near the analog circuitry.

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Absolute Maximum Ratings (*Note 1*, *Note 2*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{DDA}, V_{DDIO}	3.9V
Voltage on Any Pin to GND	−0.3V to V_{DDA} or V_{DDIO} +0.3V
Input Current on Any Pin	±25 mA
Package Input Current (*Note 3*)	±50 mA
Package Dissipation at T = 25°C	See (*Note 4*)
ESD Susceptibility	
Human Body Model (*Note 5*)	2500V
Machine Model (*Note 5*)	250V
Soldering Temperature	
Infrared, 10 sec. (*Note 6*)	235°C
Storage Temperature	−65°C to +150°C

Operating Ratings (*Note 1*, *Note 2*)

Operating Temperature Range	−40°C ≤ T_A ≤ +85°C
V_{DDA} (Supply Voltage)	+2.7V to +3.6V
V_{DDIO} (Output Driver Supply Voltage)	+2.5V to V_{DDA}
V_{REF}	1.20V
$|V_{SSA}–V_{SSIO}|$	≤ 100 mV
Clock Duty Cycle	30 to 70 %

Converter Electrical Characteristics

Unless otherwise specified, the following specifications apply for V_{SSA} = V_{SSIO} = 0V, V_{DDA} = +3.0V, V_{DDIO} = +2.5V, V_{IN} = 2 V_{P-P}, STBY = 0V, External V_{REF} = 1.20V, f_{CLK} = 40 MHz, 50% Duty Cycle, C_L = 10 pF/pin. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}**: all other limits T_A = 25°C. (*Note 9*, *Note 10*, *Note 11*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC CONVERTER CHARACTERISTICS						
	No Missing Codes Guaranteed		**10**			Bits
INL	Integral Non-Linearity	F_{IN} = 250 kHz, −0 dB Full Scale	**−1.0**	±0.3	**+1.0**	LSB
DNL	Differential Non-Linearity	F_{IN} = 250 kHz, −0 dB Full Scale	**−0.9**	±0.3	**+0.9**	LSB
GE	Gain Error	Positive Error	**−1.5**	+0.4	**+1.9**	% FS
		Negative Error	**−1.5**	−0.01	**+1.9**	% FS
OE	Offset Error (V_{IN}+ = V_{IN}−)		**−1.4**	0.12	**+1.6**	% FS
	Under Range Output Code			0		
	Over Range Output Code			1023		
FPBW	Full Power Bandwidth (*Note 16*)			400		MHz
REFERENCE AND INPUT CHARACTERISTICS						
V_{CM}	Common Mode Input Voltage		0.5		1.5	V
V_{COM}	Output Voltage for use as an input common mode voltage (*Note 8*)			1.45		V
V_{REF}	Reference Voltage			1.2		V
V_{REFTC}	Reference Voltage Temperature Coefficient			±80		ppm/°C
C_{IN}	V_{IN} Input Capacitance (each pin to V_{SSA})			4		pF
POWER SUPPLY CHARACTERISTICS						
I_{VDDA}	Analog Supply Current	STBY = 1		4.5	**6.0**	mA
		STBY = 0		18	**25**	mA
I_{VDDIO}	Digital Supply Current (*Note 14*)	STBY = 1, f_{IN} = 0 Hz		0		mA
		STBY = 0, f_{IN} = 0 Hz		0.6	**0.8**	mA
PWR	Power Consumption (*Note 15*)	STBY = 1		13.5	**18**	mW
		STBY = 0		55.5	**77**	mW

DC and Logic Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2$ V_{P-P}, STBY = 0V, External $V_{REF} = 1.20V$, $f_{CLK} = 40$ MHz, 50% Duty Cycle, $C_L = 10$ pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits $T_A = 25°C$ (*Note 9*, *Note 10*, *Note 11*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLK, DF, STBY, SENSE						
	Logical "1" Input Voltage		**2**			V
	Logical "0" Input Voltage				**0.8**	V
	Logical "1" Input Current				**+10**	µA
	Logical "0" Input Current		**−10**			µA
D0–D9 OUTPUT CHARACTERISTICS						
	Logical "1" Output Voltage	$I_{OUT} = -0.5$ mA	**V_{DDIO} − 0.2**			V
	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA			**0.4**	V
DYNAMIC CONVERTER CHARACTERISTICS (*Note 13*)						
ENOB	Effective Number of Bits	$f_{IN} = 11$ MHz	9.4, **9.3**	9.6		Bits
		$f_{IN} = 19$ MHz	9.4, **9.3**	9.6		Bits
SNR	Signal-to-Noise Ratio	$f_{IN} = 11$ MHz	58.7, **58.1**	59.6		dB
		$f_{IN} = 19$ MHz	58.6, **58**	59.5		dB
SINAD	Signal-to-Noise Ratio + Distortion	$f_{IN} = 11$ MHz	58.6, **58**	59.5		dB
		$f_{IN} = 19$ MHz	58.5, **57.8**	59.4		dB
2nd HD	2nd Harmonic	$f_{IN} = 11$ MHz	−75.9, **−74.7**	−89		dBc
		$f_{IN} = 19$ MHz	−74.4, **−73**	−86		dBc
3rd HD	3rd Harmonic	$f_{IN} = 11$ MHz	−69.5, **−67.5**	−78		dBc
		$f_{IN} = 19$ MHz	−68.8, **−66.7**	−77		dBc
THD	Total Harmonic Distortion (First 6 Harmonics)	$f_{IN} = 11$ MHz	−69.5, **−67.5**	−78		dB
		$f_{.IN} = 19$ MHz	−68.8, **−66.7**	−77		dB
SFDR	Spurious Free Dynamic Range (Excluding 2nd and 3rd Harmonic)	$f_{IN} = 11$ MHz	−75.8, **−74.5**	−80		dBc
		$f_{IN} = 19$ MHz	−75.7, **−74.3**	−80		dBc

AC Electrical Characteristics

Unless otherwise specified, the following specifications apply for $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2 V_{P-P}$ (full scale), STBY = 0V, External $V_{REF} = 1.20V$, $f_{CLK} = 40$ MHz, 50% Duty Cycle, $C_L = 10$ pF/pin. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}:** all other limits $T_A = 25°C$ ([*Note 10*](), [*Note 11*](), [*Note 12*]())

Symbol	Parameter	Conditions	Min ([*Note 12*]())	Typ ([*Note 12*]())	Max ([*Note 12*]())	Units
CLK, DF, STBY, SENSE						
$f_{CLK}1$	Maximum Clock Frequency				40	MHz (min)
$f_{CLK}2$	Minimum Clock Frequency			20		MHz
t_{CH}	Clock High Time			12.5		ns
t_{CL}	Clock Low Time			12.5		ns
t_{CONV}	Conversion Latency				**6**	Cycles
t_{OD}	Data Output Delay after a Rising Clock Edge	T = 25°C	2	3.3	5	ns
			1		**6**	ns
t_{AD}	Aperture Delay			1		ns
t_{AJ}	Aperture Jitter			2		ps (RMS)
	Over Range Recovery Time	Differential V_{IN} step from ±3V to 0V to get accurate conversion		1		Clock Cycle
t_{STBY}	Standby Mode Exit Cycle			20		Cycles

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = $V_{SSA} = V_{SSIO} = 0V$, unless otherwise specified.

Note 3: When the voltage at any pin exceeds the power supplies ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A)/\theta_{JA}$. In the 28-pin TSSOP, θ_{JA} is 96°C/W, so $P_D MAX = 1,302$ mW at 25°C and 677 mW at the maximum operating ambient temperature of 85°C. Note that the power dissipation of this device under normal operation will typically be about 55.5 mW. The values for maximum power dissipation listed above will be reached only when the ADC10040 is operated in a severe fault condition.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through 0Ω.

Note 6: The 235°C reflow temperature refers to infrared reflow. For Vapor Phase Reflow (VPR) the following conditions apply: Maintain the temperature at the top of the package body above 183°C for a minimum of 60 seconds. The temperature measured on the package body must not exceed 220°C. Only one excursion above 183°C is allowed per reflow cycle.

Note 7: The analog inputs are protected as shown below. Input voltage magnitude up to 500 mV beyond the supply rails will not damage this device. However, input errors will be generated if the input goes above V_{DDA} or V_{DDIO} and below V_{SSA} or V_{SSIO}.
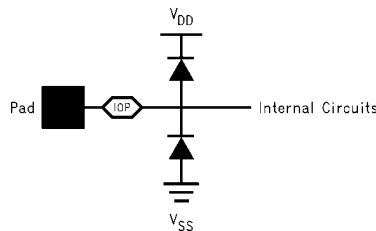
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Note 8: V_{COM} is a typical value, measured at room temperature. It is not guaranteed by test. Do not load this pin.

Note 9: To guarantee accuracy, it is required that $|V_{DDA} - V_{DDIO}| \leq 100$ mV and separate bypass capacitors are used at each power supply pin.

Note 10: With the test condition for 2 V_{P-P} differential input, the 10-bit LSB is 1.95 mV.

Note 11: Typical figures are at $T_A = T_J = 25°C$ and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 12: Timing specifications are tested at TTL logic levels, $V_{IL} = 0.4V$ for a falling edge, and $V_{IH} = 2.4V$ for a rising edge.

Note 13: Optimum dynamic performance will be obtained by keeping the reference input in the +1.2V.

Note 14: V_{DDIO} is the current consumed by the switching of the output drivers and is primarily determined by load capacitance on the output pins, the supply voltage, V_{DR}, and the rate at which the outputs are switching (which is signal dependent). $I_{DR} = V_{DR} \times (C_0 \times f_0 + C_1 \times f_1 + C_2 + f_2 + ... C_{11} \times f_{11})$ where V_{DR} is the 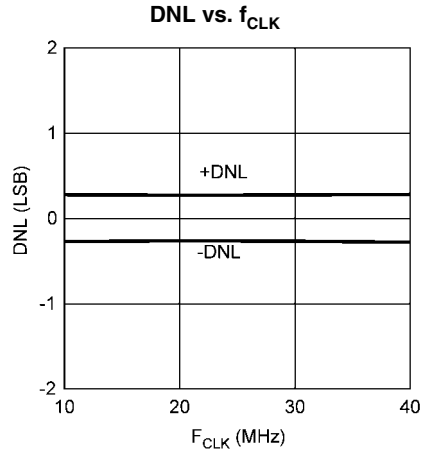output driver supply voltage, C_n is the total load capacitance on the output pin, and f_n is the average frequency at which the pin is toggling.

Note 15: Power consumption includes output driver power. ($f_{IN} = 0$ MHz).

Note 16: The input bandwidth is limited using a capacitor between V_{IN-} and V_{IN+}.

Specification Definitions

APERTURE DELAY is the time after the rising edge of the clock to when the input signal is acquired or held for conversion.

APERTURE JITTER (APERTURE UNCERTAINTY) is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. potential present at both signal inputs to the ADC.

CONVERSION LATENCY See PIPELINE DELAY.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the ADC clock input signal.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as (SINAD - 1.76) / 6.02 and states that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated as:

Gain Error = Pos. Full-Scale Error – Neg. Full-Scale Error

INTEGRAL NON LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC10040 is guaranteed not to have any missing codes.

NEGATIVE FULL SCALE ERROR is the difference between the input voltage ($V_{IN+} - V_{IN-}$) just causing a transition from negative full scale to the first code and its ideal value of 0.5 LSB.

OFFSET ERROR is the input voltage that will cause a transition from a code of 01 1111 1111 to a code of 10 0000 0000.

OUTPUT DELAY is the time delay after the rising edge of the clock before the data update is presented at the output pins.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available at the output pins the Pipeline Delay plus the Output Delay after the sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POSITIVE FULL SCALE ERROR is the difference between the actual last code transition and its ideal value of 1½ LSB below positive full scale.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD) Is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dBc, of the rms total of the first six harmonic levels at the output to the level of the fundamental at the output. THD is calculated as:

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + \ldots + f_{10}^2}{f_1^2}}$$

where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_6 are the RMS power in the first 6 harmonic frequencies.

SECOND HARMONIC DISTORTION (2ND HARM) is the difference expressed in dB, between the RMS power in the input frequency at the output and the power in its 2nd harmonic level at the output.

THIRD HARMONIC DISTORTION (3RD HARM) is the difference, expressed in dB, between the RMS power in the input frequency at the output and the power in its 3rd harmonic level at the output.

Timing Diagram
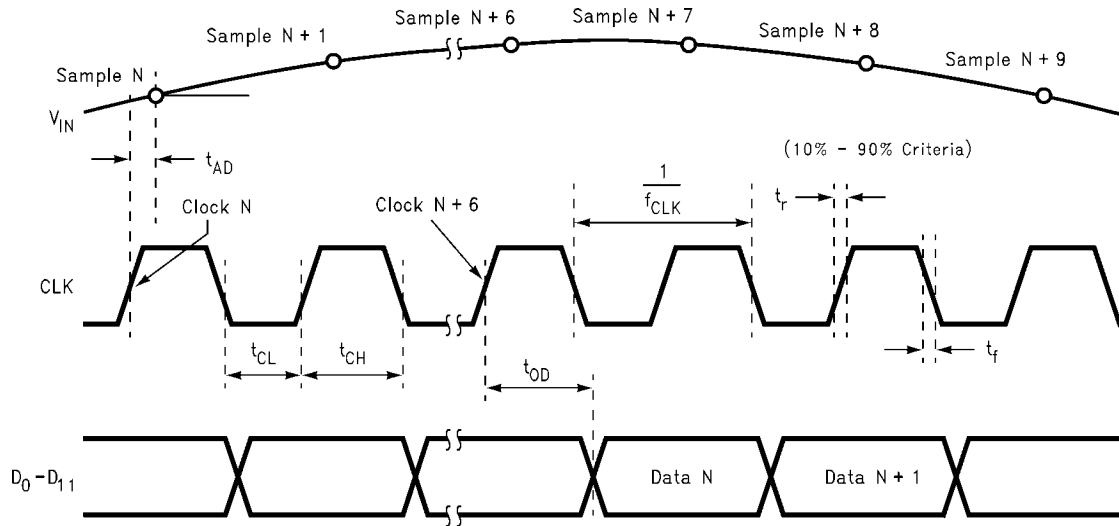
FIGURE 1. Clock and Data Timing Diagram

Transfer Characteristics
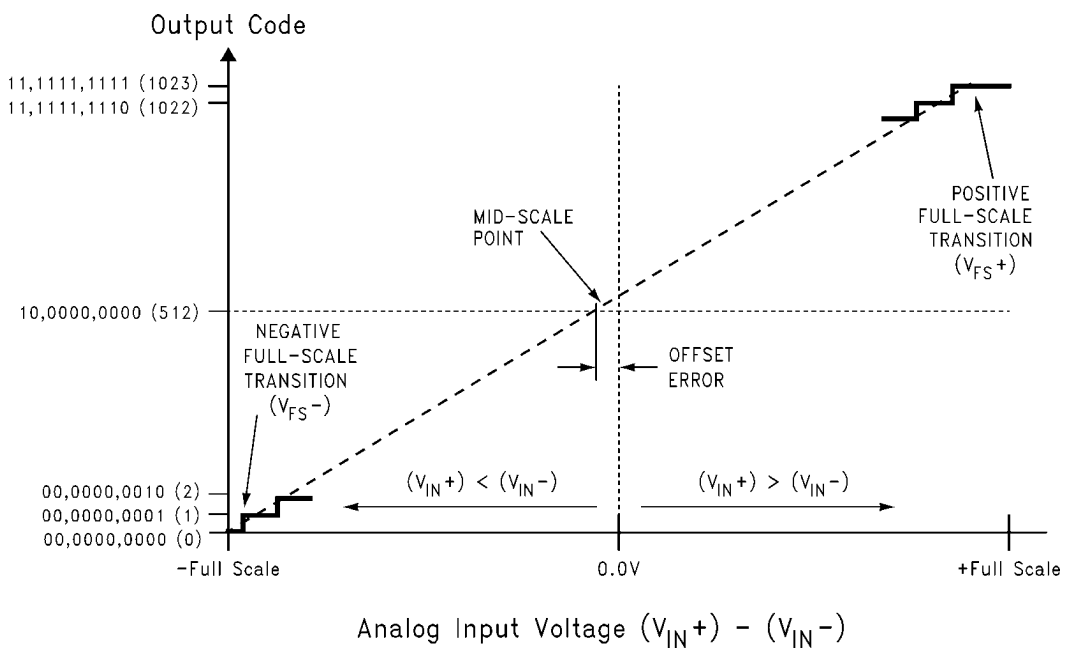
FIGURE 2. Input vs. Output Transfer Characteristic

Typical Performance Characteristics
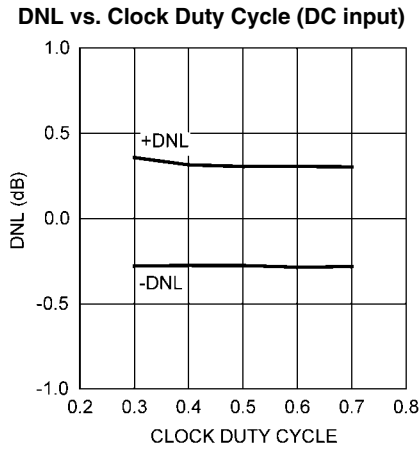Unless otherwise specified, the following specifications apply: $V_{SSA} = V_{SSIO} = 0V$, $V_{DDA} = +3.0V$, $V_{DDIO} = +2.5V$, $V_{IN} = 2 V_{P-P}$, STBY = 0V, External $V_{REF} = 1.2V$, $f_{CLK} = 40$ MHz, $f_{IN} = 19$ MHz, 50% Duty Cycle.
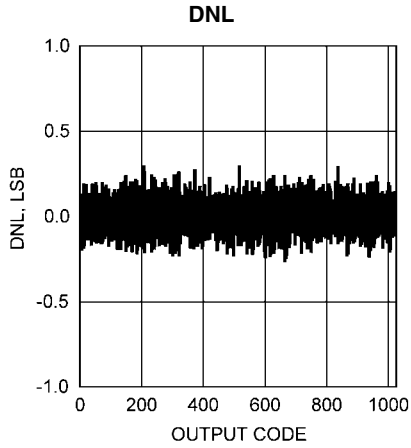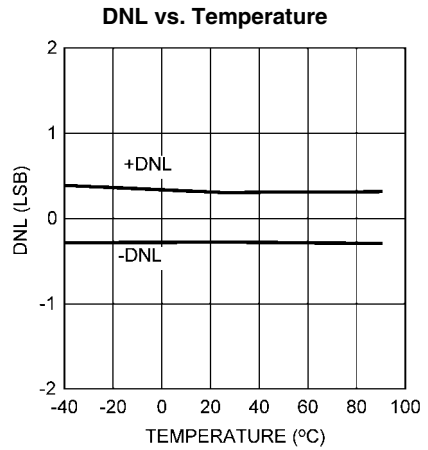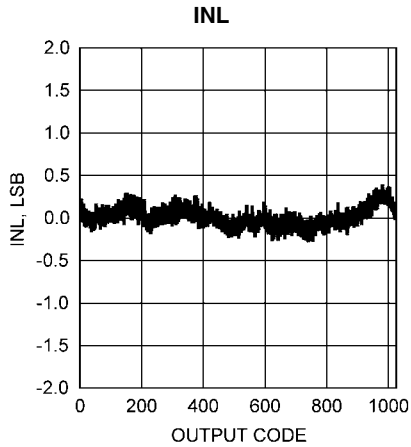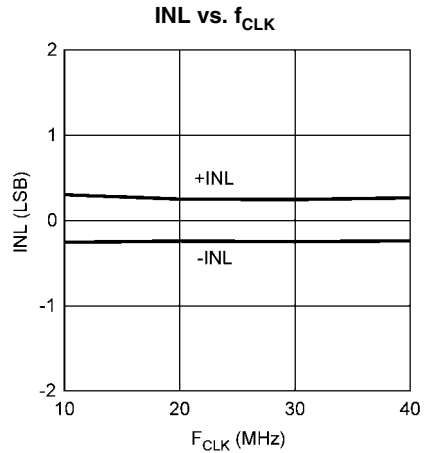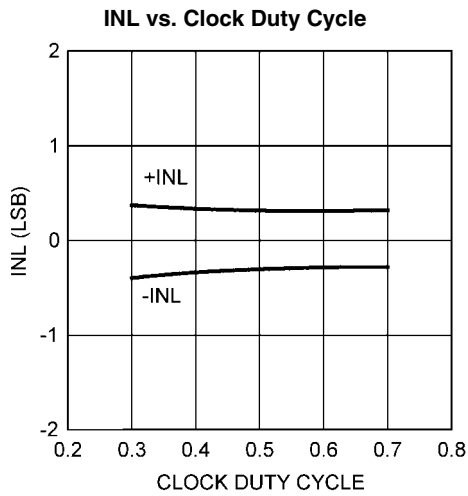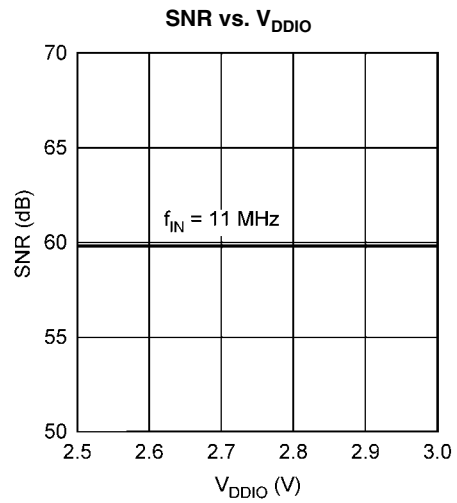
DNL

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DNL vs. f_{CLK}

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DNL vs. Clock Duty Cycle (DC input)

20077813

DNL vs. Temperature

20077816

INL

20077814

INL vs. f_{CLK}

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INL vs. Clock Duty Cycle

20077818

SNR vs. V_DDIO

20077819

SNR vs. V_DDA

20077820

SNR vs. f_CLK

20077821

INL vs. Temperature

20077822

SNR vs. Clock Duty Cycle

20077823

SNR vs. Temperature

20077824

THD vs. V_{DDA}

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THD vs. V_{DDIO}

20077826

THD vs. f_{CLK}

20077827

SNR vs. IRS

20077828

THD vs. IRS

20077829

SINAD vs. V_DDA

20077830

SINAD vs. V_DDIO

20077831

THD vs. Clock Duty Cycle

20077832

SINAD vs. Clock Duty Cycle

20077833

THD vs. Temperature

20077834

SINAD vs. Temperature

20077835

SINAD vs. f_{CLK}

20077836

SFDR vs. V_{DDIO}

20077837

SINAD vs. IRS

20077838

SFDR vs. f_{CLK}

20077839

SFDR vs. V_{DDA}

20077840

SFDR vs. IRS

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SFDR vs. Clock Duty Cycle

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Spectral Response @ 11 MHz Input

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SFDR vs. Temperature

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Spectral Response @ 19 MHz Input
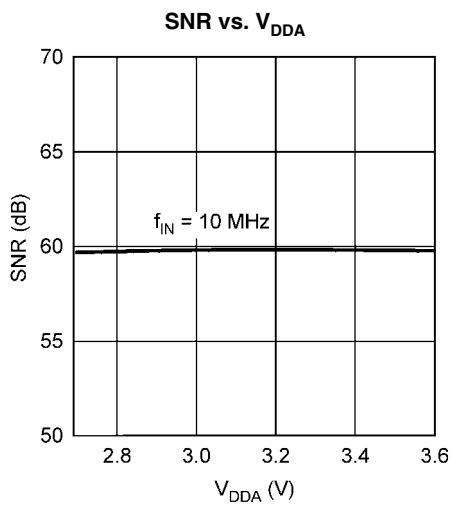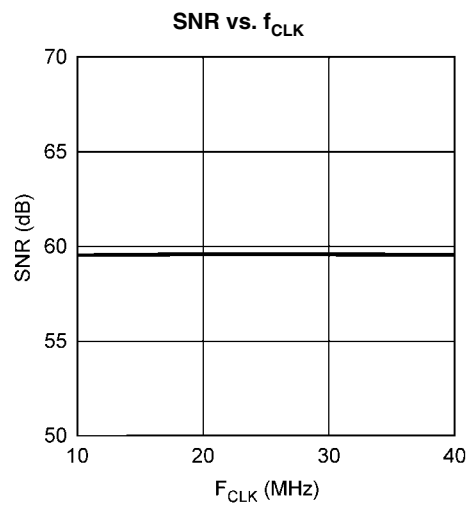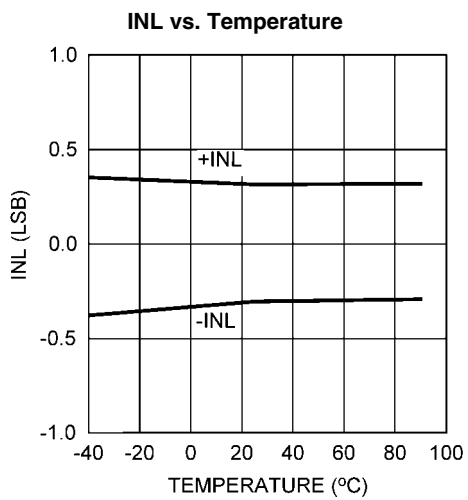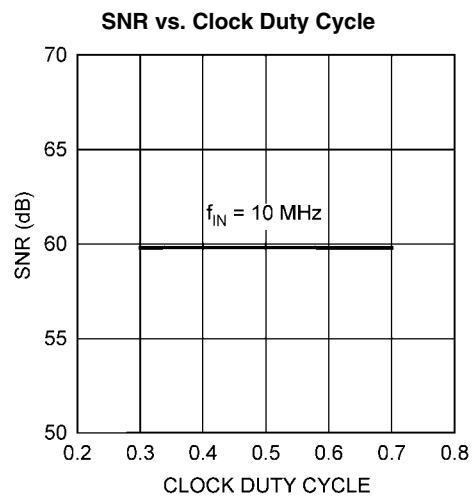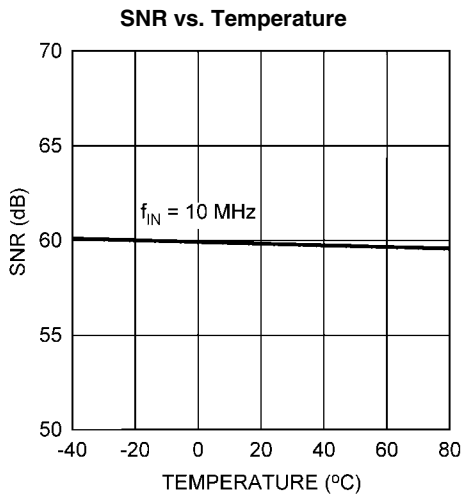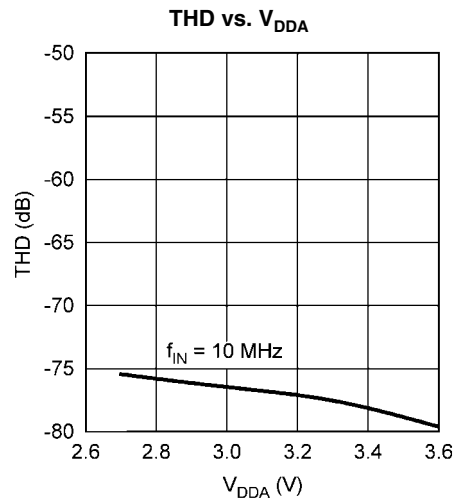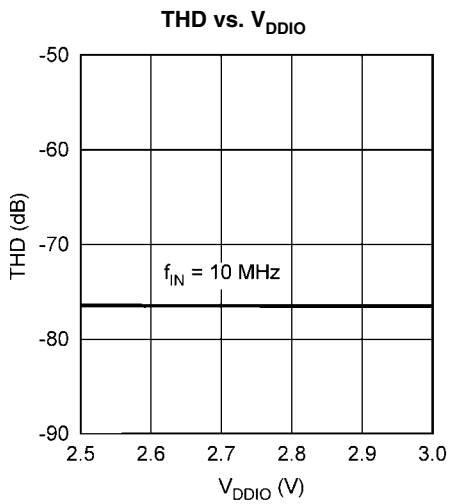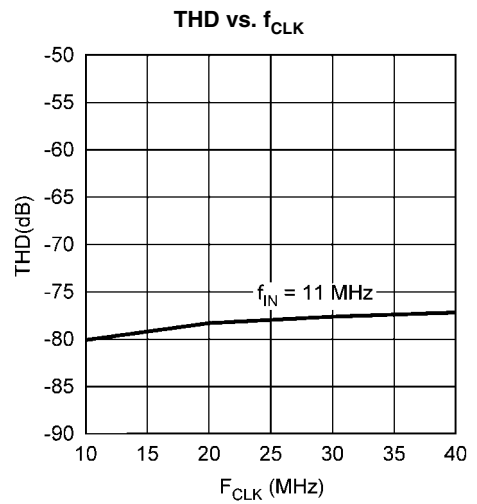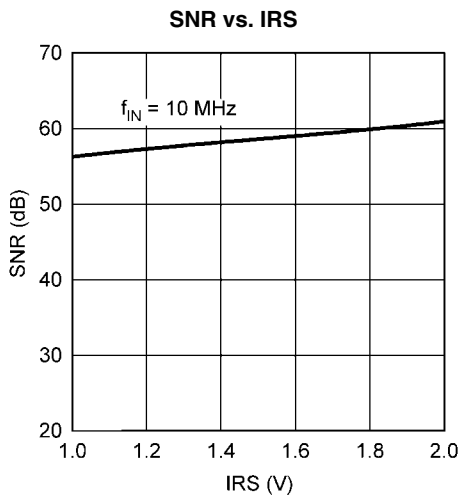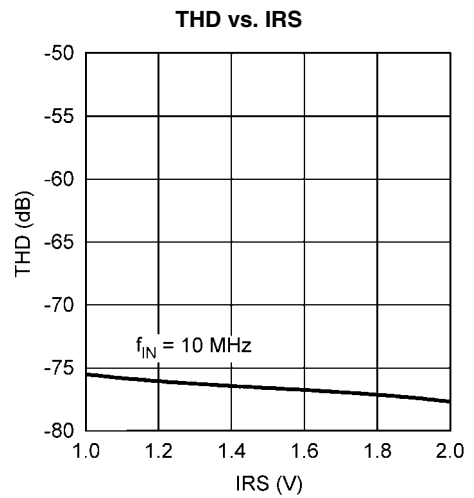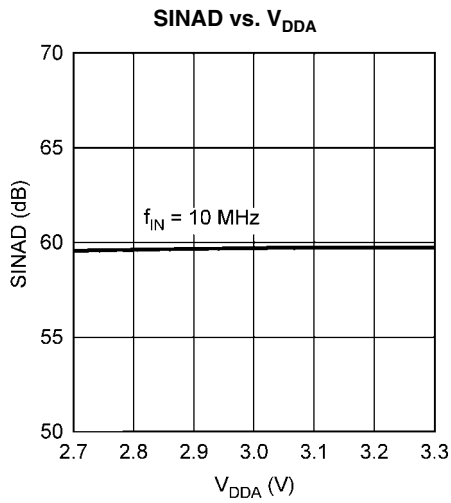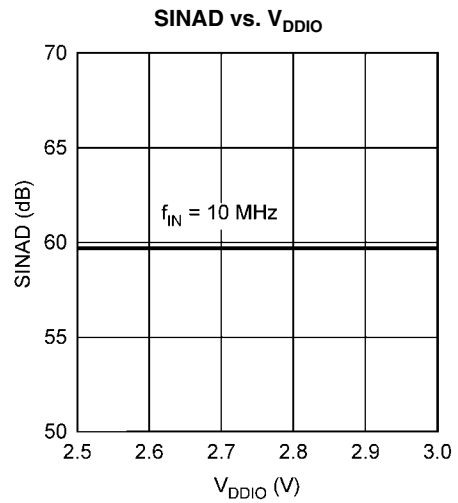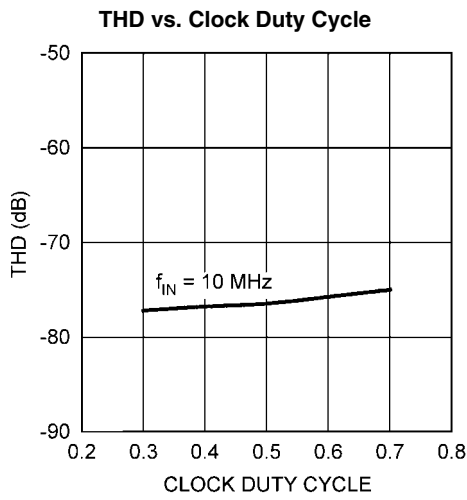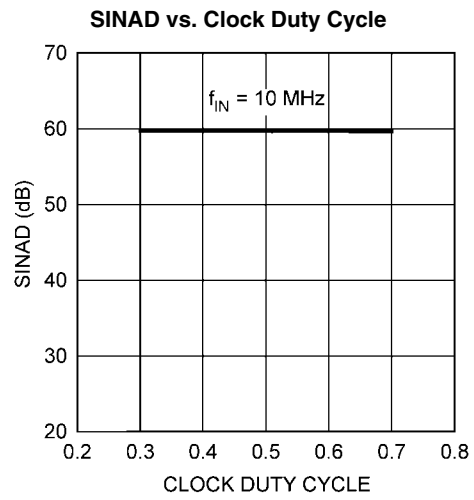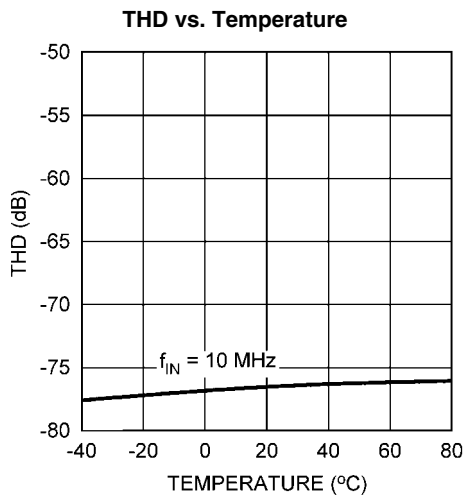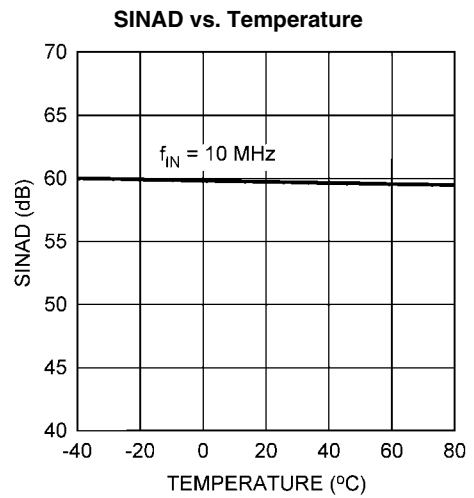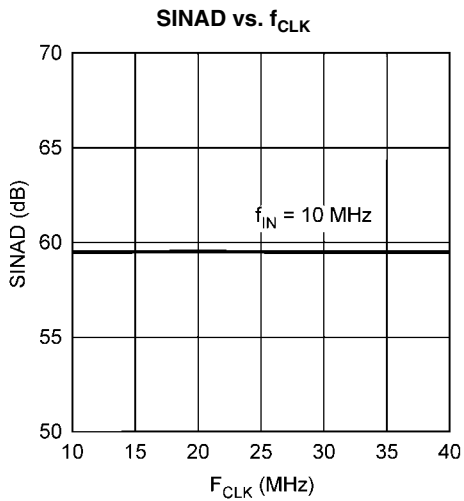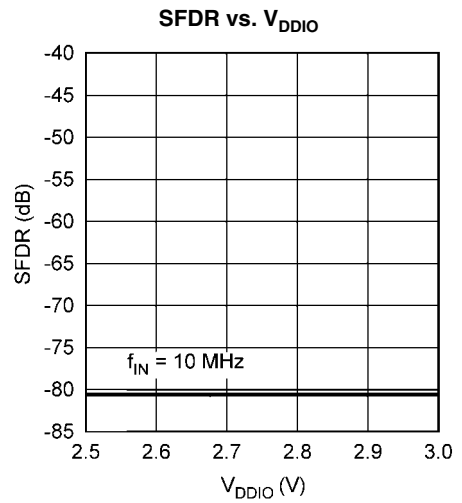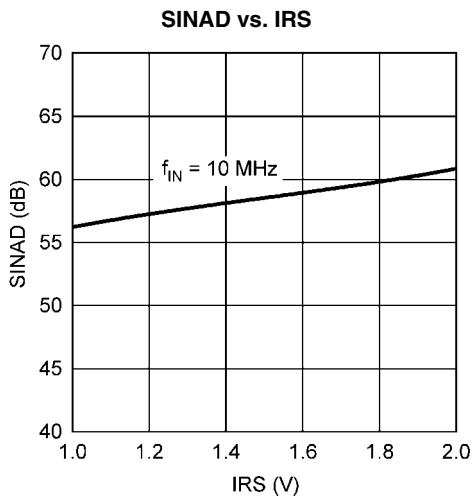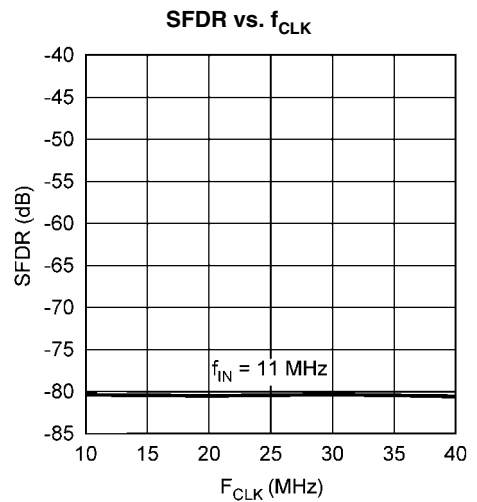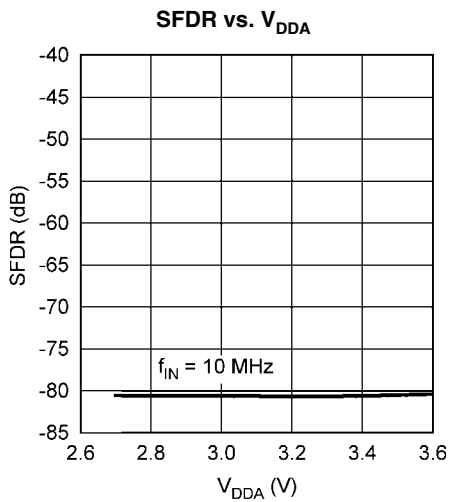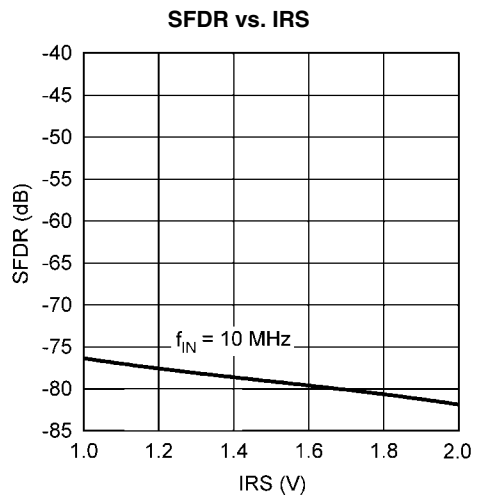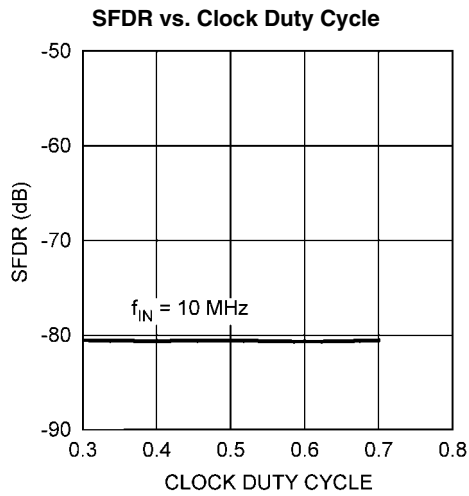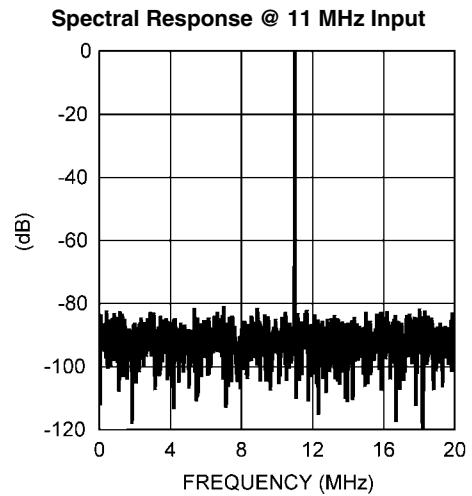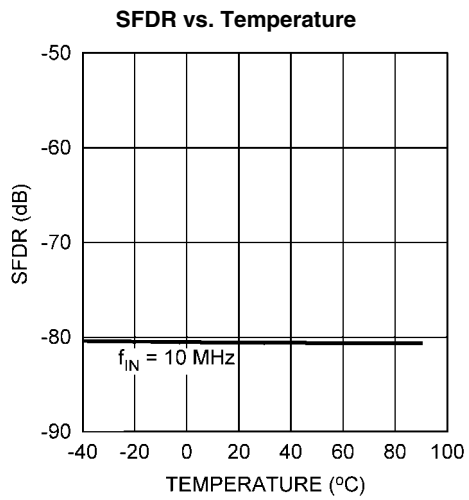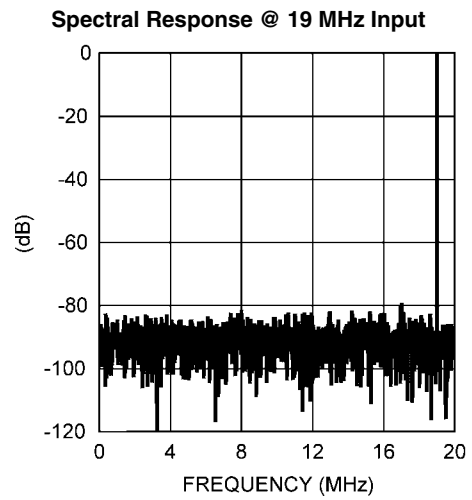
20077845

Functional Description

The ADC10040 uses a pipeline architecture and has error correction circuitry to help ensure maximum performance. Differential analog input signals are digitized to 10 bits. In differential mode , each analog input signal should have a peak-to-peak voltage equal to 1.0V, 0.75V or 0.5V, depending on the state of the IRS pin (pin 5), and be centered around V_{CM} and be 180° out of phase with each other. If single ended operation is desired, V_{IN}- may be tied to the V_{COM} pin (pin 4). A single ended input signal may then be applied to V_{IN}+, and should have an average value in the range of V_{CM}. The signal amplitude should be 2.0V, 1.5V or 1.0V peak-to-peak, depending on the state or the IRS pin (pin 5).

Applications Information

1.0 ANALOG INPUTS

The ADC10040 has two analog signal inputs, V_{IN}+ and V_{IN}−. These two pins form a differential input pair. There is one common mode pin V_{COM} that may be used to set the common mode input voltage.

1.1 REFERENCE PINS

The ADC10040 is designed to operate with an internal or external 1.2V reference. The internal 1.2V reference is the default condition. If an external voltage is applied to the V_{REF} pin, then that voltage is used for the reference. The V_{REF} pin should be bypassed to ground with a 0.1 µF capacitor placed close to the pin. Do not load this pin when using the internal reference.

The voltages at V_{COM}, V_{REFT}, and V_{REFB} are derived from the reference voltage. These pins are made available for bypass purposes only. These pins should each be bypassed to ground with a 0.1 µF capacitor placed close to the pin. It is very important that all grounds associated with the reference voltage and the input signal make connection to the analog ground plane at a single point to minimize the effects of noise currents in the ground path. DO NOT LOAD these pins.

1.2 V_{COM} PIN

This pin supplies a voltage for possible use to set the common mode input voltage. This pin may also be connected to V_{IN}-, so that V_{IN}+ may be used as a single ended input. These pins should be bypassed with at least a 0.1uF capacitor. Do not load this pin.

1.3 SIGNAL INPUTS

The signal inputs are V_{IN}+ and V_{IN}−. The input signal amplitude is defined as V_{IN}+ − V_{IN}− and is represented schematically in *Figure 3*:
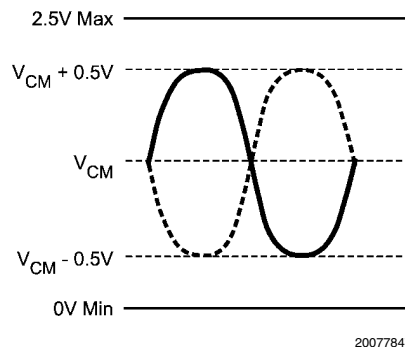
FIGURE 3. Input Voltage Waveforms for a 2V$_{P-P}$ differential Input
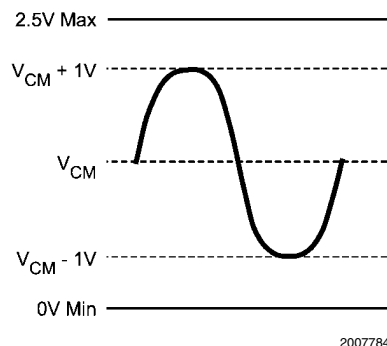
FIGURE 4. Input Voltage Waveform for a 2V$_{P-P}$ Single Ended Input

A single ended input signal is shown in *Figure 4*.

The internal switching action at the analog inputs causes energy to be output from the input pins. As the driving source tries to compensate for this, it adds noise to the signal. To minimize the effects of this, use 18Ω series resistors at each of the signal inputs with a 25 pF capacitor across the inputs, as shown in *Figure 5*. These components should be placed close to the ADC because the input pins of the ADC is the most sensitive part of the system and this is the last opportunity to filter the input. The two 16Ω resistors and the 24 pF capacitor, together with the 4 pF ADC input capacitance, form a low-pass filter with a -3 dB frequency of 177 MHz.

1.4 CLK PIN

The CLK signal controls the timing of the sampling process. Drive the clock input with a stable, low jitter clock signal in the frequency range indicated in the AC Electrical Characteristics Table with rise and fall times of less than 2 ns. The trace carrying the clock signal should be as short as possible and should not cross any other signal line, analog or digital, not even at 90°. The CLK signal also drives an internal state machine. If the CLK is interrupted, or its frequency is too low, the charge on internal capacitors can dissipate to the point where the accuracy of the output data will degrade. This is what limits the lowest sample rate. The duty cycle of the clock signal can affect the performance of any A/D Converter. Because achieving a precise duty cycle is difficult, the ADC10040 is designed to maintain performance over a range of duty cycles. While it is specified and performance is guaranteed with a 50% clock duty cycle, performance is typically maintained with minimum clock low and high times indicated in the AC Electrical Characteristics Table. Both minimum high and low times may not be held simultaneously.

1.5 STBY PIN

The STBY pin, when high, holds the ADC10040 in a power-down mode to conserve power when the converter is not being used. The power consumption in this state is 13.5 mW. The output data pins are undefined in this mode. Power consumption during power-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in the power down.

1.6 DF PIN

The DF (Data Format) pin, when high, forces the ADC10040 to output the 2's complement data format. When DF is tied low, the output format is offset binary.

1.7 IRS PIN

The IRS (Input Range Select) pin defines the input signal amplitude that will produce a full scale output. The table below describes the function of the IRS pin.

TABLE 1. IRS Pin Functions

IRS Pin	Full-Scale Input
V_{DDA}	$2.0V_{P-P}$
V_{SSA}	$1.5V_{P-P}$
Floating	$1.0V_{P-P}$

1.8 OUTPUT PINS

The ADC10040 has 10 TTL/CMOS compatible Data Output pins. The offset binary data is present at these outputs while the DF and STBY pins are low. Be very careful when driving a high capacitance bus. The more capacitance the output drivers must charge for each conversion, the more instanta-neous digital current flows through V_{DDIO} and V_{SSIO}. These large charging current spikes can cause on-chip noise and couple into the analog circuitry, degrading dynamic performance. Adequate bypassing, limiting output capacitance and careful attention to the ground plane will reduce this problem. Additionally, bus capacitance beyond the specified 10 pF/pin will cause t_{OD} to increase, making it difficult to properly latch the ADC output data. The result could be an apparent reduction in dynamic performance. To minimize noise due to output switching, minimize the load currents at the digital outputs. This can be done by minimizing load capacitance and by connecting buffers between the ADC outputs and any other circuitry, which will isolate the outputs from trace and other circuit capacitances and limit the output currents, which could otherwise result in performance degradation. Only one driven input should be connected to the ADC output pins.

While the t_{OD} time provides information about output timing, a simple way to capture a valid output is to latch the data on the rising edge of the conversion clock.

1.9 APPLICATION SCHEMATICS

The following figures show simple examples of using the ADC10040. The ADC10040 performs best with a differential input signal.

1.9.1 Narrow Band A.C. Signals

Figure 5 shows a typical circuit for an AC coupled, differentially driven input. The 16Ω resistors and 24 pF capacitor, together with the 4 pF input capacitance of the ADC10040, provides a –3dB input bandwidth of 177 MHz, while the 0.1µF capacitor at V_{COM} stabilizes the common move voltage at the transformer center tap.
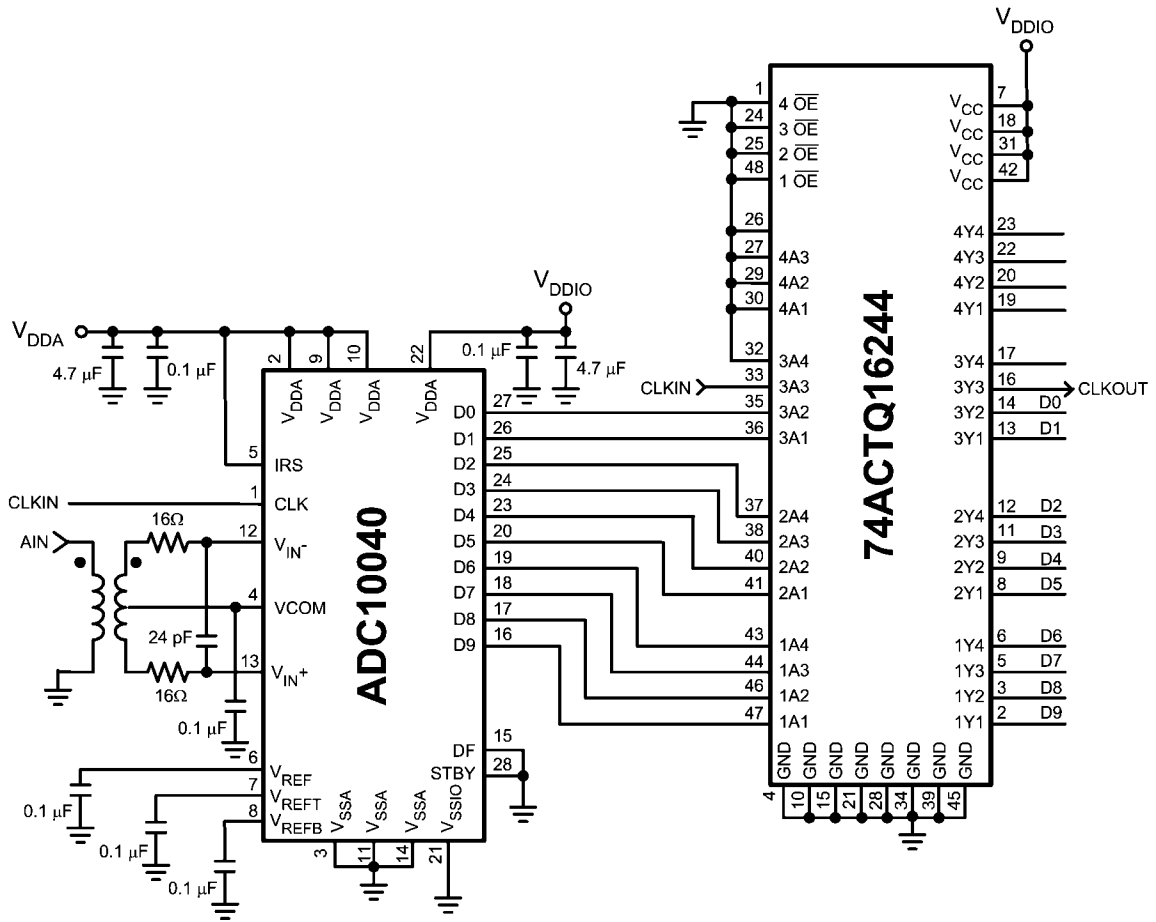
FIGURE 5. A Simple Application Using a Differential Signal Source

1.9.2 D.C. Applications

For very low frequency and DC input applications, a d.c. coupled amplifier or buffer may be needed, especially when the input is single-ended and the advantages of a differential input signal is desired. *Figure 6* shows the input drive circuit that can be used to replace the transformer of *Figure 5*. The LMH6550 provides excellent performance and is well-suited for this application. The common mode output voltage of the LMH6550 is the same as its VCM input.
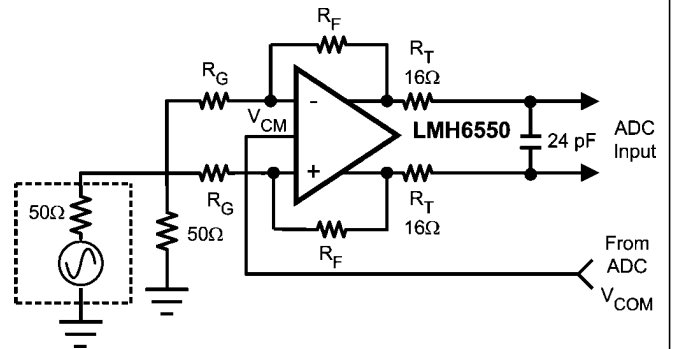
FIGURE 6. Using the LMH6550 for DC and wideband applications

1.9.3 Single Ended Applications

Performance of the ADC10040 with a single-ended input is not as good as its performance with a differential input. However, if the lower performance is adequate, the circuit of *Figure 7* shows an acceptable method of driving the analog input.
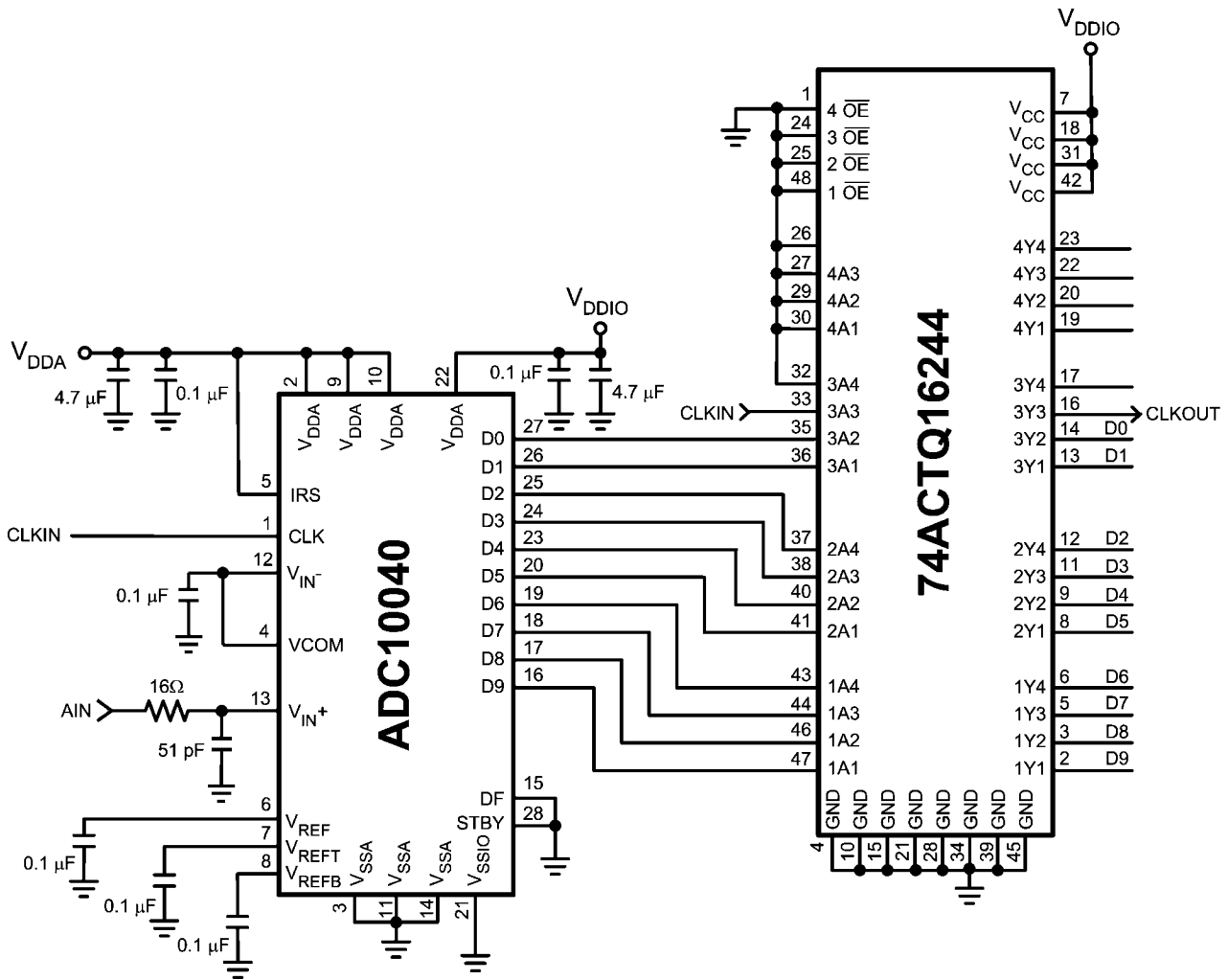
FIGURE 7. A Simple Application Using a Single Ended Signal Source

20077850

ADC10040/ADC10040Q

Physical Dimensions inches (millimeters) unless otherwise noted

9.7±0.1

6.4

3.2

4.4±0.1

0.2 A B⑤ C⑤
ALL LEAD TIPS
2 PLACES

PIN #1 ID

1.1 MAX
TYP

0.1 A

A

28X 0.19-0.30
0.1Ⓜ A B⑤ C⑤

26X 0.65

DIMENSIONS ARE IN MILLIMETERS

SYMM ℄

SYMM ℄

(5.94)
TYP

(4.16)
TYP

(1.78)
TYP

(28X 0.42)
(26X 0.65)

LAND PATTERN RECOMENDATION

(0.9)

0.1±0.05
TYP

SEE DETAIL A

0.09-0.20 TYP

R0.09 MIN
R0.09 MIN

0°-8°

0.6±0.1

(12°) TOP & BOTTOM

GAGE PLANE

0.25

SEATING PLANE

(1)

DETAIL A
TYPICAL
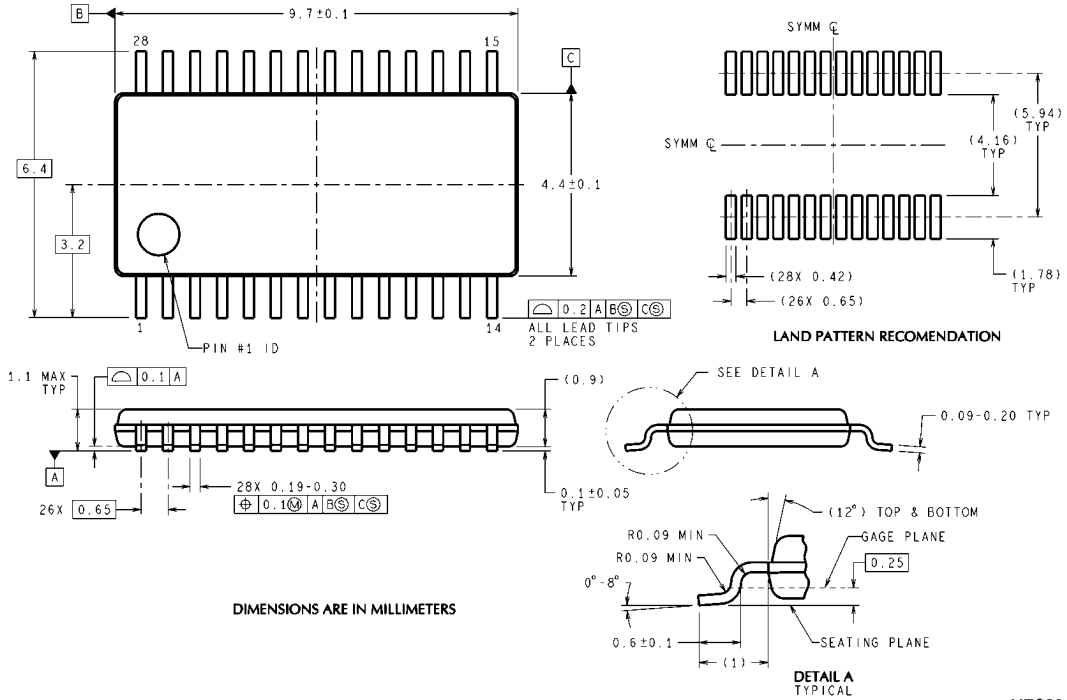
MTC28 (Rev D)

28-Lead TSSOP Package
Ordering Number ADC10040CIMT, ADC10040QCIMT
NS Package Number MTC28

Notes

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Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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