HEWLETT PACKARD

Silicon Bipolar Monolithic Dual Conversion Vector Modulator with Phase Shifter

Technical Data

HPMX-2004

Features

- **On Board Active Digital Phase Shifter**
- **I/Q Bandwidth > 10 MHz**
- **Wide Bandwidth:**
  1st LO, 40-240 MHz
  2nd LO, 250-2250 MHz
  RF Output, 250-2000 MHz
- **On Chip Mixer for Dual Conversion**
- **Low Power Dissipation:**
  Standby, 120 µW
  Operating, 150 mW
- **Low Cost Plastic Surface Mount Package**

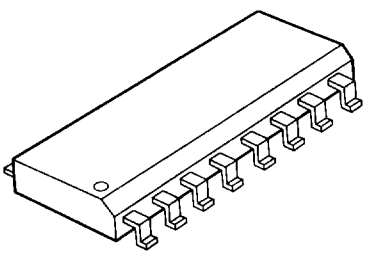
Applications

- **Digital Cellular and Cordless Telephones such as NADC, JDC, GSM, PCN, and PHP**
- **Wireless LANs**
- **RF Data Links**
- **Vector Generators**

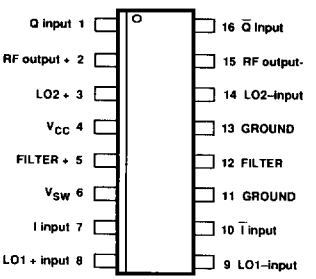
Description

The HPMX-2004 is a silicon monolithic, dual conversion, quadrature modulator in a plastic, surface mount SO- 16 package.

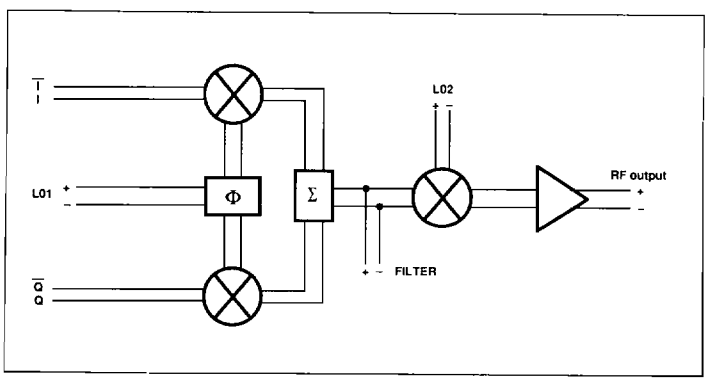
Plastic S0-16 Package



HPMX-2004 Pinout



Functional Block Diagram



At the time this catalog was printed, this product was not yet released for sale. Please contact the local HP Field Sales Office for more information. All specifications are subject to change.

The dual conversion architecture and wide band nature of the Gilbert cells allows operation over a broad range of frequencies with little change in performance. A low gain output stage is used to achieve a wide bandwidth with 50 Ω match.

All signal inputs and outputs except V_{SW} are differentially balanced with RF ports matched to 50 Ω, and can be used balanced or unbalanced in any combination. Double balanced mixers are used to improve port to port isolation and reduce harmonic content in the output signal.

I and Q inputs are internally biased and have high input impedances to allow them to be driven from high impedance sources. either AC or DC coupled.

All on-chip circuitry is biased by a set of current sources controlled by the standby circuit. When activated, the standby circuit turns all the current sources off, reducing current drain to only 25 μA, the current required by the standby circuit alone.

This device is manufactured using Hewlett-Packard's 13 GHz f_T, 25 GHz f_{MAX} silicon bipolar integrated circuit process.

HPMX-2004 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	HPMX-2004
V_{CC}	Device Voltage, T_{case} = 25°C	Volts	6
V_{in} I/Q	I/Q Input Voltage	V_{p-p}	4
P_{in} LO	Local Oscillator Input Power	dBm	+10
V_{sw}	Standby Mode Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

*Operation in excess of any one of these conditions may result in permanent damage to this device. Care should be taken to prevent electrostatic discharge (ESD) that could permanently damage the device. This device has a Class 1 ESD rating.

Thermal Resistance: HPMX-2004 Thermal Resistance, Junction to Ambient, Θ_{ja} = 160°C/W

Notes:
1. Junction temperature can be determined by $T_j = (P_d \times \Theta_{ja}) + T_a$.
2. Maximum soldering temperature is 260°C for 5 seconds.

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Electrical Parameters, T_A = 25°C, V_{CC} = 5 V

Symbol	Parameters/Test Conditions: LO1 = - 7 dBm @ 100 MHz, LO2 = -3 dBm @ 900 MHz, I/Q = 1.2 V_{p-p} @ 70 kHz, Z_o = 50 Ω, Test Circuit #1 (unless otherwise noted)	Units	Typical
I_{cc}	Power Supply Current	mA	30
I_{cc}	Standby Current, V_{sw} = +3.0 V	mA	21
	I/Q Input Impedance (Internally Biased with High Impedance Source to ≈ 2.5 VDC)	Ohms pF	8,000 1.0
	LO1 Operating Frequency Range	MHz	40 to 240
	LO2 Operating Frequency Range	MHz	250 to 2,000
	I/Q Modulating Frequency Range	MHz	DC to 10
	RF Output Frequency Range	MHz	250 to 2,000
T_{on}	Turn-On Time, to ± 0.5 dB of Final Output Power (Test Circuit #4)	µS	1.2
T_{off}	Turn-Off Time, to Output Power Below Noise Floor (Test Circuit #4)	µS	0.4

800 MHz RF Electrical Parameters, T_A = 25°C, V_{CC} = 5 V

Symbol	Parameters/Test Conditions: LO1 = - 7 dBm @ 100 MHz, LO2 = -3 dBm @ 900 MHz, I/Q = 1.2 V_{p-p} differential @ 70 kHz, Z_o = 50 Ω, Test Circuit #2 (unless otherwise noted)		Units	Typical
P_{out}	RF Output Power @ 800 MHz		dBm	-13.0
	RF Output Power Flatness, 800-1000 MHz		dB	± 0.6
P_{1dB}	Power Output at 1 dB Compression Point (I/Q voltage swept)		dBm	-12.5
LO1 P_{in}	LO1 Power Input for Phase Shift of 90° ± 3°		dBm	-7
Noise	Output Noise Floor		dBm/Hz	-136
	Modulation Product Power Levels in dB Relative to the Desired Sideband Using Filter at 1st Carrier Output	Residual LO (800 MHz) Undesired Sideband (799.93 MHz) 2nd Harmonic (800 ± 0.140 MHz) 3rd Harmonic (800 ± 0.210 MHz) 5th Harmonic (800 ± 0.350 MHz)	dBc dBc dBc dBc dBc	-34 -41 -49 -53 -72
	LO1 Input SWR		VSWR	2.0:1
	LO2 Input SWR		VSWR	1.2:1
	RF Output SWR (operating)		VSWR	1.5:1
A_i	I/Q Amp. Imbalance (derived from undesired sideband data)		dB	± 0.15
P_i	I/Q Phase Imbalance (derived from undesired sideband data)		Deg.	± 0.97

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