HEWLETT PACKARD

Silicon Bipolar Monolithic Conversion Quadrature Modulator

Technical Data

HPMX-2002

Features

- **I/Q Bandwidth >10 MHz**
- **Wide Bandwidth**
  1st LO, 40-300 MHz
  2nd LO, 250-2,000 MHz
  RF 250-2,000 MHz
- **On Chip Mixer for Dual Conversion**
- **Low Power Dissipation**
  Standby, 50 µW
  Operating, 60 mW
- **Low Cost Plastic Surface Mount Package**

Applications

- **Digital Cellular Radio**
- **RF Data Links**
- **Vector Generators**

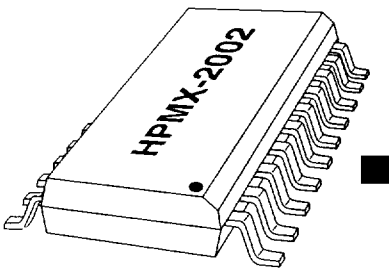
Description

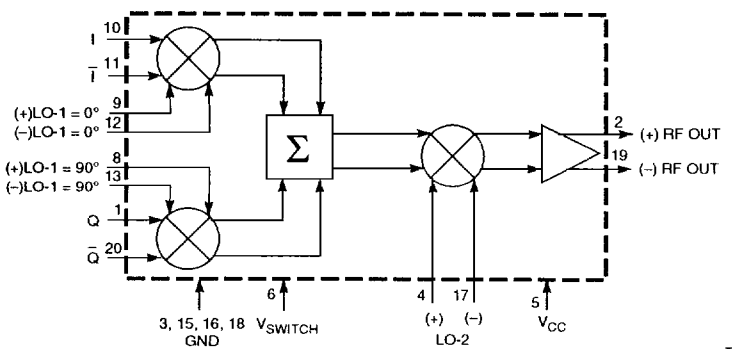
The HPMX-2002 is a silicon monolithic, dual conversion, quadrature modulator in a plastic surface mount SO-20 package. It has typical LO-1 operating frequency range of 40-300 and LO-2 of 250-2,000 MHz, and typical I/Q bandwidth of >10 MHz.

The LO inputs are self biased and have 50 Ohm termination impedances. The RF output has a -11 dBm output power level. The HPMX-2002 also features a standby mode in which the device consumes only 11 µA of current.

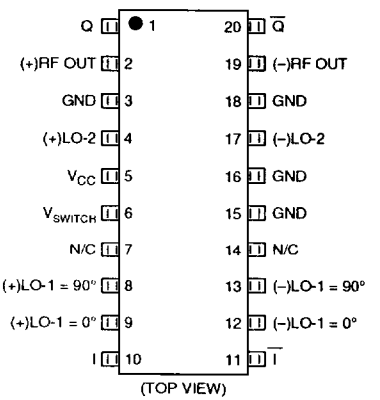
The device is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Plastic SO-20 Package





Functional Block Diagram



Pin Configuration

Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Max.
V_{cc}	Supply Voltage	Volts	6
V_{in} I/Q	I/Q Input Voltage	Volts P-P	4
P_{in} L/O	Lo Input Power	dBm	+10
V_{switch}	Standby Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

* Operation in excess of any one of these conditions may result in permanent damage to this device. Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. Class I device.

Notes:

1. A θ_{ja} of 200°C/W should be used for derating and junction temperature calculations:
   $T_j = (P_d \times \theta_{ja}) + T_A$
2. Maximum soldering temperature is 260°C for 5 seconds.

RF Electrical Parameters, T_A = 25°C, V_{CC} = 5V

Symbol	Parameter/Test Condition: LO-1 = -14 dBm F = 100 MHz, LO-2 = -3 dBm F = 900 MHz, I/Q = 70 kHz 1.2V P-P (Differential), Z_O = 50 Ohms, Test Circuit #2		Units	Min.	Typ.	Max.
P_{out}	RF Output Power at 800 MHz		dBm		-11	
	RF Output Power Flatness, 800 to 1,000 MHz		dB		±0.6	
P_{1dB}	Power Out at 1 dB Compression (I/Q Voltage Swept)		dBm		-12.5	
Noise	Output Noise Floor		dBm/Hz		-136	
	Modulation product power levels in dB relative to the desired sideband with filter at 1st carrier output	Residual L/O (800 MHz) [1]	dBc		-38	-30
		Undesired Sideband (799.93 MHz)[2]	dBc		-52	-30
		2nd Harmonic (800 ± 0.140 MHz)[3]	dBc		-47	-30
		3rd Harmonic (800 ± 0.210 MHz)[3]	dBc		-42	-30
		5th Harmonic (800 ± 0.350 MHz)[3]	dBc		-57	-50
	LO-1 Input SWR		SWR		1.5:1	
	LO-2 Input SWR		SWR		1.2:1	
	RF Output SWR (Operating)		SWR		1.5:1	
A_i	I/Q Amplitude Imbalance (Derived from undesired sideband data)		dB		0.04	
P_i	I/Q Phase Imbalance (Derived from undesired sideband data)		Deg.		0.25	

Notes:

1. Residual LO = (F_{LO2} - F_{LO1})
2. Undesired Sideband = (F_{LO2} - F_{LO1} - F_{IQ})
3. Nth Harmonic = (F_{LO2} - F_{LO1}) ± (N * F_{IQ})

Electrical Parameters, T_A = 25°C, V_{CC} = 5V

Symbol	Parameter/Test Condition: LO-1 = -14 dBm F=100 MHz, LO-2 = -3 dBm F = 900 MHz, I/Q = 70 kHz 1.2V P-P Z_o = 50 Ohms, Test Circuit #1 (unless noted)	Units	Typ.	Max.
I_{cc}	Supply Current	mA	12.2	15
I_{cc}	Standby Current, V_{switch} = +3.0 V	µA	10.5	15
	I/Q Input Impedance (Internally Biased with High Impedance Source to ≅ 2.3 Volts DC)	Ohms pF	8K 1.0	
	LO-1 Operating Frequency Range	MHz	40 to 300	
	LO-2 Operating Frequency Range	MHz	250 to 2,000	
	I/Q Modulating Frequency Range	MHz	DC to 10	
	RF Output Frequency Range	MHz	250 to 2,000	
T_{on}	Turn-on Time, within 0.5 dB Final Output Power (Test Circuit #4)	µs	1.2	
T_{off}	Turn-off Time, Output Power below Noise Floor (Test Circuit #4)	µs	0.4	

Theory of Operation

Figure 1 shows the simplified block diagram of the HPMX-2002. The device consists of 3 double balanced active "Gilbert cell" mixers and two amplifier stages. I and Q inputs are mixed with the LO-1 0° and LO-1 90° signals respectively. These signals are then amplified, level shifted, up-converted, and fed to the output through an amplifier stage.

Double balanced mixers are used to improve port isolation and reduce spurious signals at the output. All signal inputs (except V_{switch}) are differentially balanced and RF ports are matched to 50 Ohms. I and Q inputs have high impedances to ensure that they can be driven from high impedance sources. All of the signal inputs can be used either single endedly or differentially with proper terminations.

The mixers and amplifiers use current sources that are controlled by the standby circuit. When the standby circuit is activated, the control line turns off the current sources for all subcells. The remaining power dissipation is due only to the standby circuit.

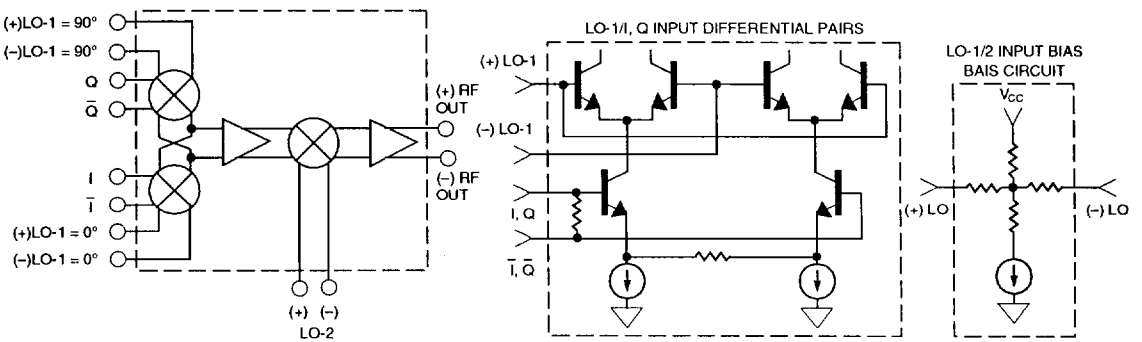


Figure 1. HPMX-2002 Simplified Schematic

High Frequency Performance

The dual conversion architecture and the wideband nature of the Gilbert cell allows an excellent performance to 2 GHz. The output stage gain has been kept low which gives wide bandwidth to allow this device to be used over a wide range of LO-2 frequencies. For equal input signals, harmonic suppression will generally improve at higher LO-2 frequencies. RF performance at 1.9 GHz is similar to performance at 800 MHz but with reduced output power.

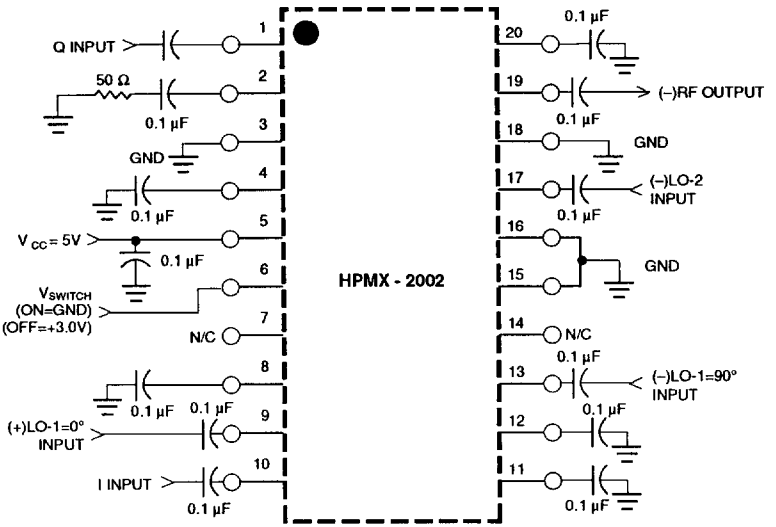


Figure 2. HPMX-2002 Test Circuit #1, Broadband Operation

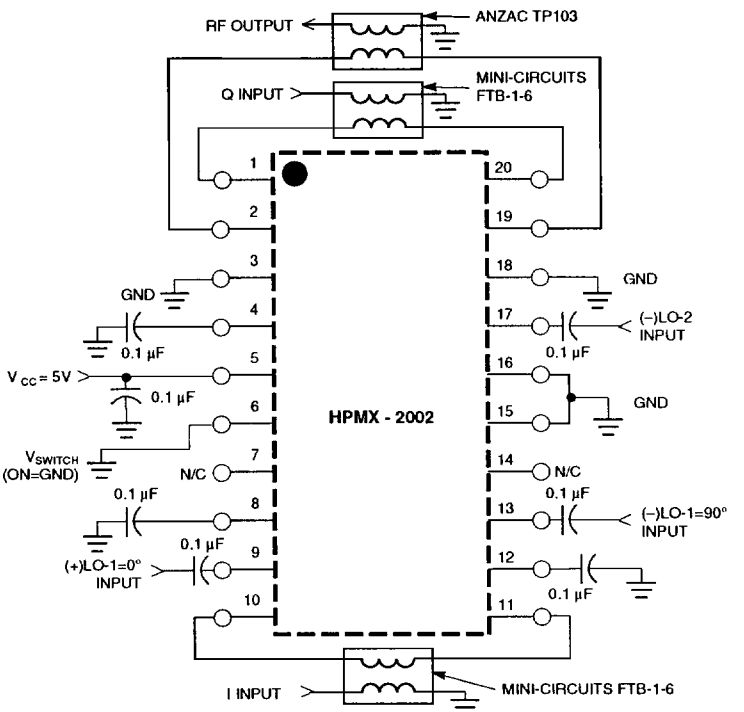


Figure 3. HPMX-2002 Test Circuit #2, Differential Operation

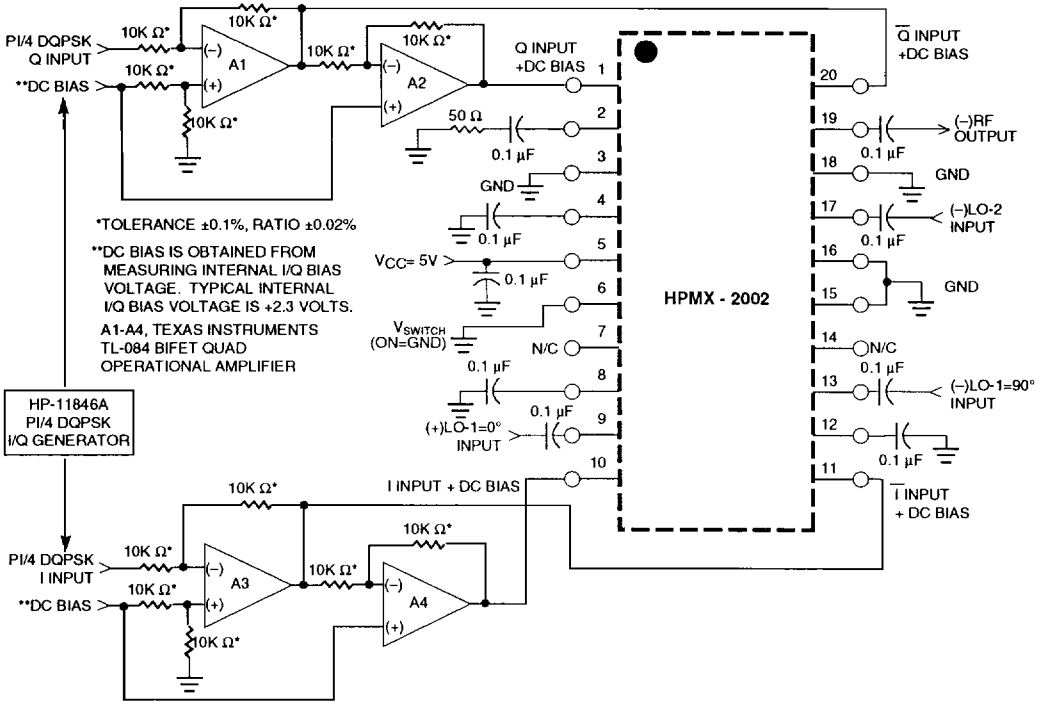


Figure 4. HPMX-2002 Test Circuit #3, Spectral Mask.

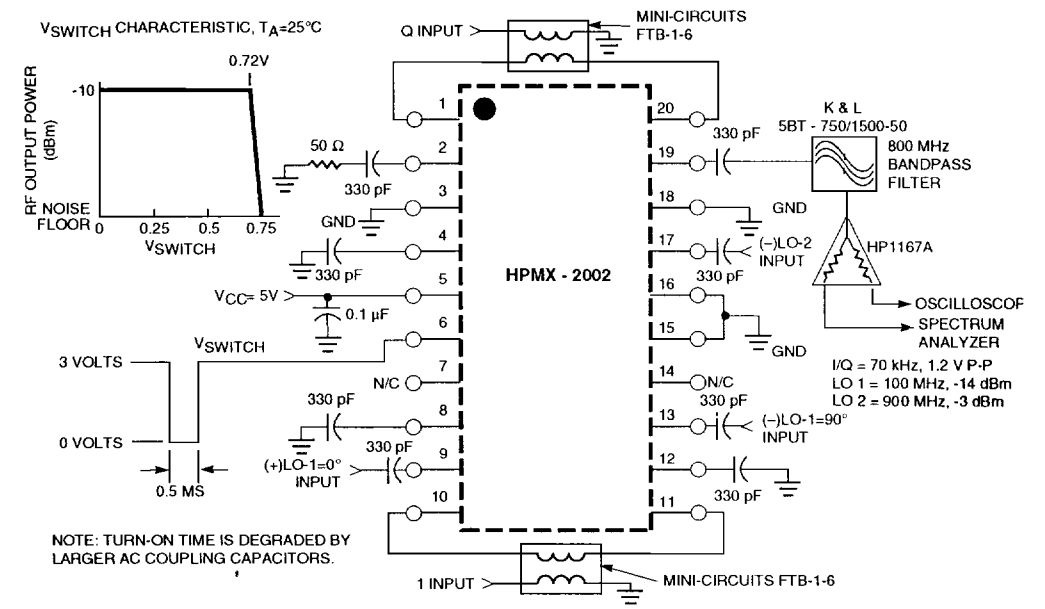


Figure 5. HPMX-2002 Test Circuit #4, Turn-On Time.

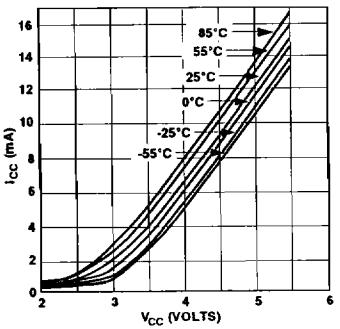


Figure 6. Typical I_{CC} vs. V_{CC} vs. Temperature

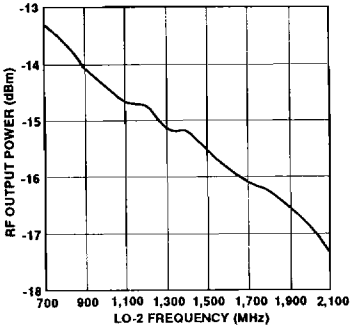


Figure 7. Typical RF Output Frequency Response; LO-1 = -14 dBm at 100 MHz: LO-2 = -3dBm: I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

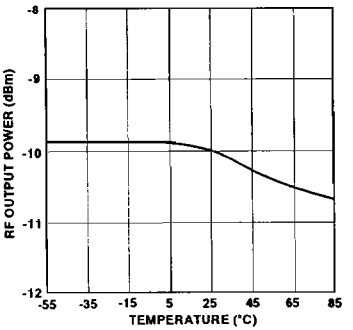


Figure 8. Typical Output Power at 800.07 MHz vs. Temperature; LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

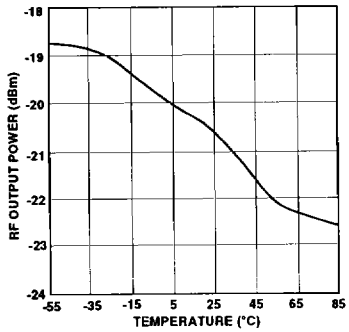


Figure 9. Typical Output Power at 800.07 MHz vs. Temperature; LO-1 = -28 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

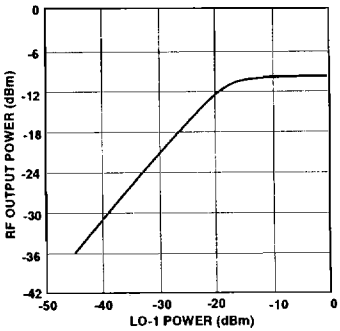


Figure 10. Typical Output Power at 800.07 MHz vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

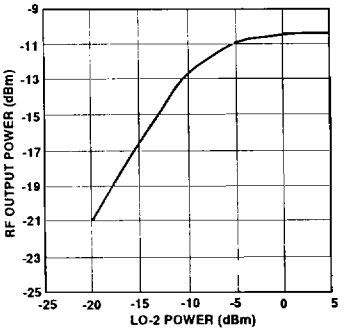


Figure 11. Typical Output Power at 800.07 MHz vs. LO-2 Power; LO-1 = -14 dBm at 100 MHz; LO-2 = 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #2

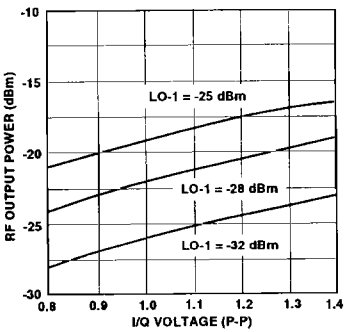


Figure 12. Typical Output Power vs. I/Q Voltage vs. LO-1 Power; LO-1 at 100 MHz; LO-2 = -3dBm at 900 MHz; Test Circuit #2

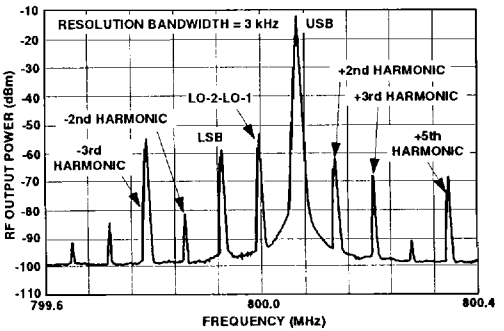


Figure 13. Typical Output Frequency Spectrum, LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

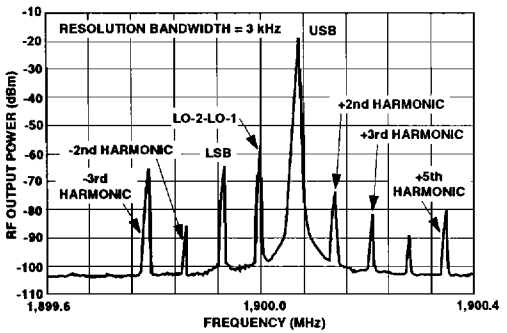


Figure 14. Typical Output Frequency Spectrum, LO-1 = -14 dBm at 100 MHz; LO-2 = -3dBm at 2,000 MHz; I/Q = 70 kHz, 1.2 V P-P; Test Circuit #1

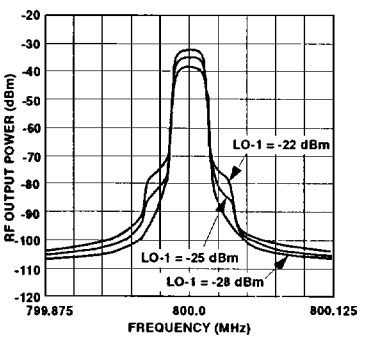


Figure 15. Typical Output Spectral Mask vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz; I/Q = 1.2 Volts P-P; π/4 DQPSK, PRBS = 20; Symbol Clock = 24.3 kHz; Test Circuit #3

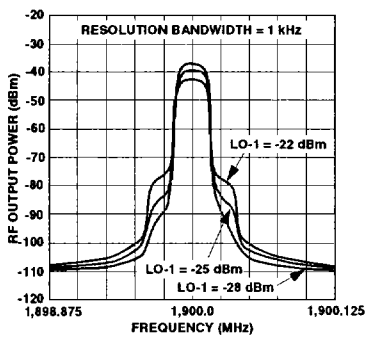


Figure 16. Typical Output Spectral Mask vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3 dBm at 2,000 MHz; I/Q = 1.2 Volts P-P; π/4 DQPSK, PRBS = 20; Symbol Clock = 24.3 kHz, Test Circuit #3

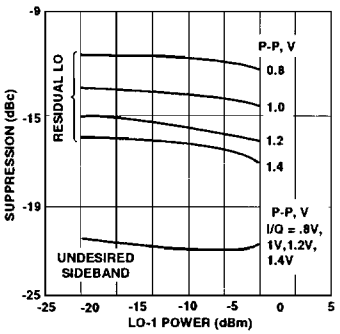


Figure 17. Typical Residual LO and Undesired Sideband Suppression at 800 MHz vs. LO-1 Power vs. I/Q Voltage; LO-1 = 100 MHz; LO-2 = -3 dBm; at 900 MHz, LO-2 = -3 dBm at 900 MHz, I/Q = 70 kHz, Test Circuit #2

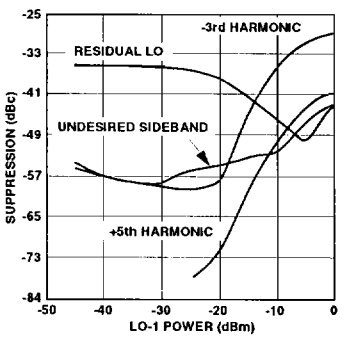


Figure 18. Typical Undesired Sideband, Residual LO, and Harmonic Suppression at 800 MHz vs. LO-1 Power; LO-1 = 100 MHz; LO-2 = -3dBm at 900 MHz, I/Q = 70 kHz, 1.2 Volts P-P; Test Circuit #2

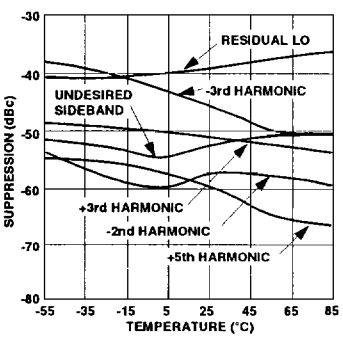


Figure 19. Typical Residual LO, Undesired Sideband and Harmonic Suppression at 800 MHz, LO-1 = -14 dBm at 100 MHz; LO-2 = -3 dBm at 900 MHz; I/Q = 1.2 Volts P-P, π/4 DQPSK; PRBS = 20, Symbol Clock = 24.3 kHz; Test Circuit #3

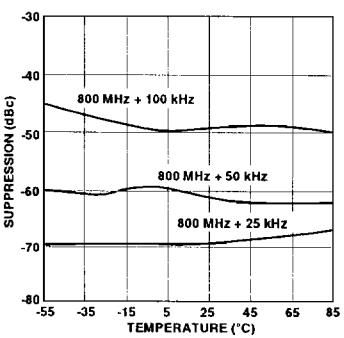
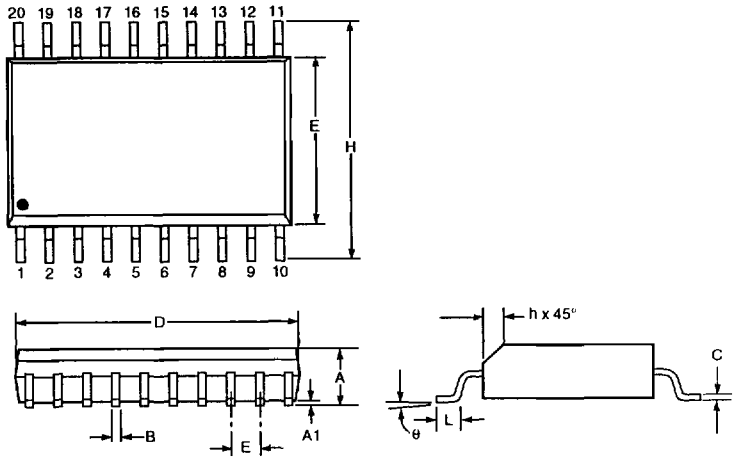


Figure 20. Typical Spectral Mask IMD/ Noise Suppression vs. Temperature; LO-1 = -28 dBm at 100 MHz; LO-2 = -3 dBm at 900 MHz; I/Q = 1.2 Volts P-P, π/4 DQPSK; PRBS = 20, Symbol Clock = 24.3 kHz; Test Circuit #3

Package Dimensions

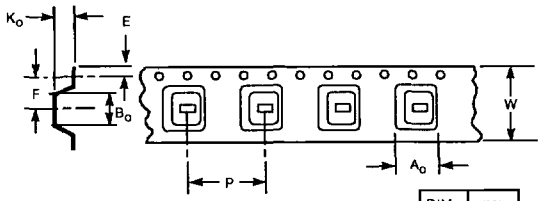
Plastic SO-20 Package

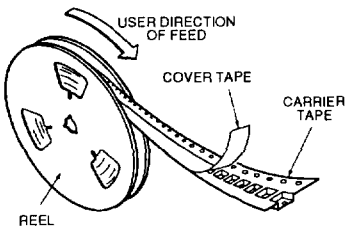


SYMBOL	DIMENSIONS MIN.	DIMENSIONS MAX.
A	2.35 (0.093)	2.65 (0.104)
A1	0.10 (0.004)	0.30 (0.012)
B	0.35 (0.014)	0.49 (0.019)
C	0.23 (0.009)	0.31 (0.012)
D	12.6 (0.496)	13.0 (0.512)
E	7.40 (0.291)	7.60 (0.299)
e	1.27 BSC (0.050)	
H	10.26 (0.404)	10.65 (0.419)
h	0.50 (0.020)	0.75 (0.030)
L	0.86 (0.034)	1.07 (0.042)
θ	0	8

MEETS JEDEC OUTLINE DIMENSIONS.
DIMENSIONS ARE IN MILLIMETERS (INCHES).

SOIC-20L Carrier Tape - HPMX-2002





DIM.	mm
W	24
P	12
A_o	10.9
B_o	13.3
K_o	3.0
E	1.75
F	11.5

TOLERANCE ±0.10

Device Orientation