

2SJ278

Silicon P Channel MOS FET

REJ03G0856-0200
(Previous: ADE-208-1190)
Rev.2.00
Sep 07, 2005

Description

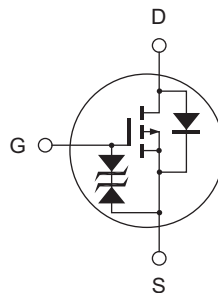
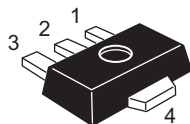
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for switching regulator, DC-DC converter

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK[®])



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "MY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	-1	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-4	A
Body to drain diode reverse drain current	I _{DR}	-1	A
Channel dissipation	P _{ch} ^{Note 2}	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value on the alumina ceramic board (12.5 × 20 × 0.7 mm)

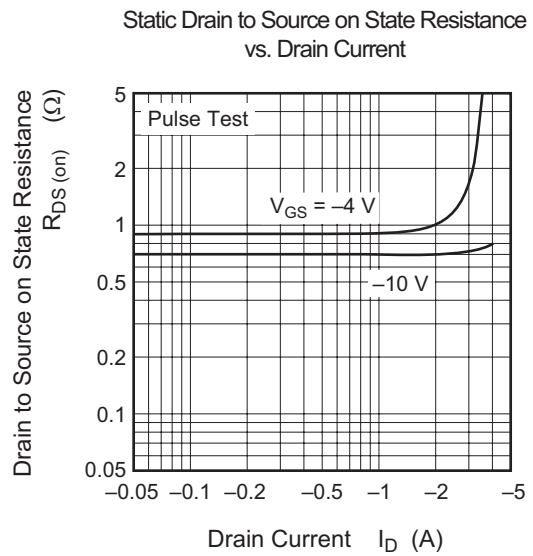
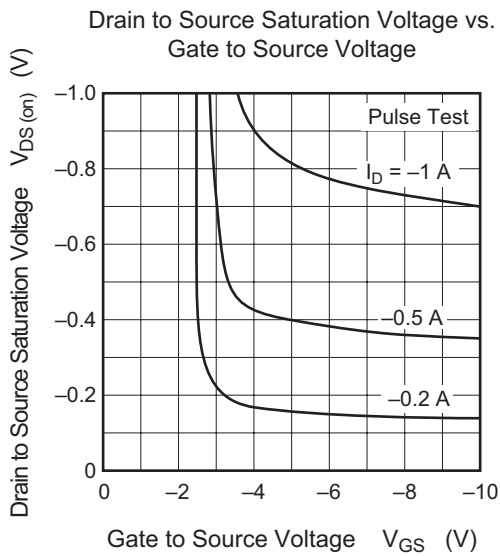
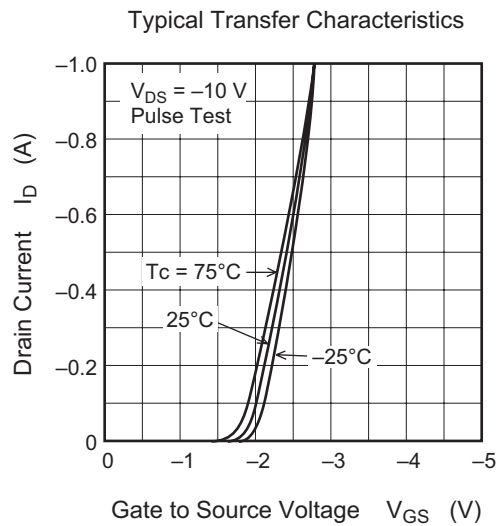
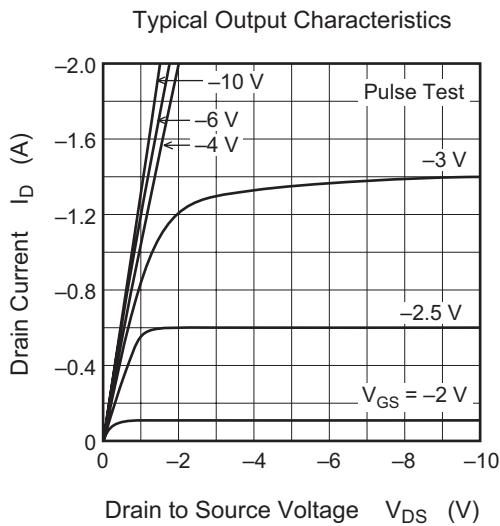
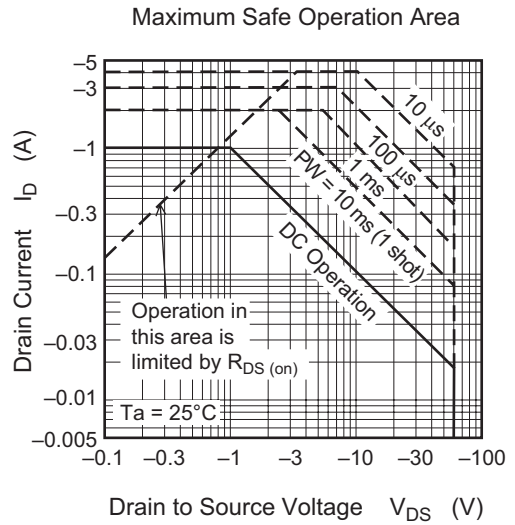
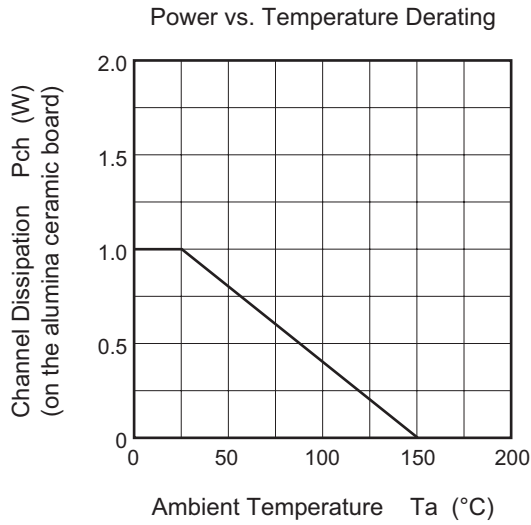
Electrical Characteristics

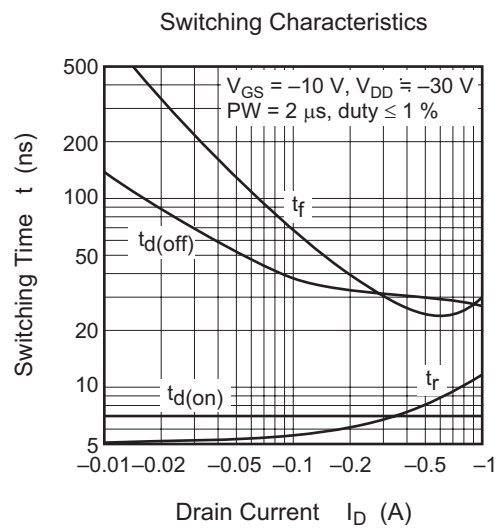
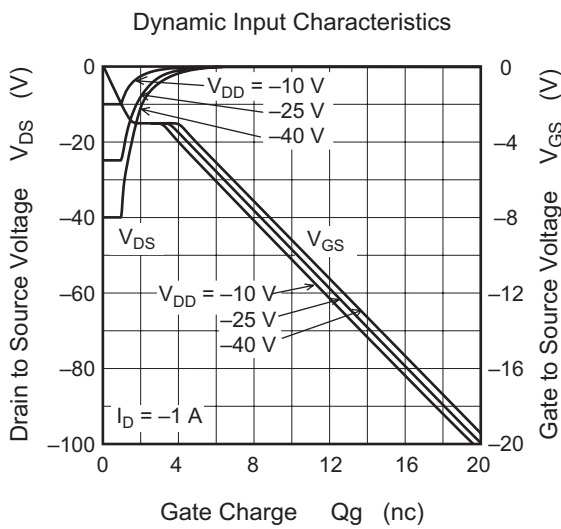
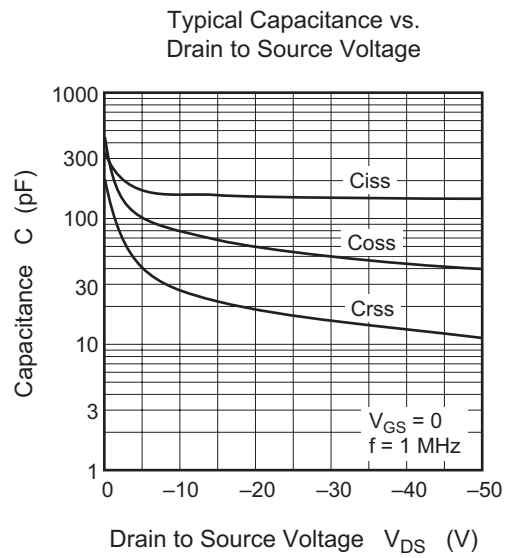
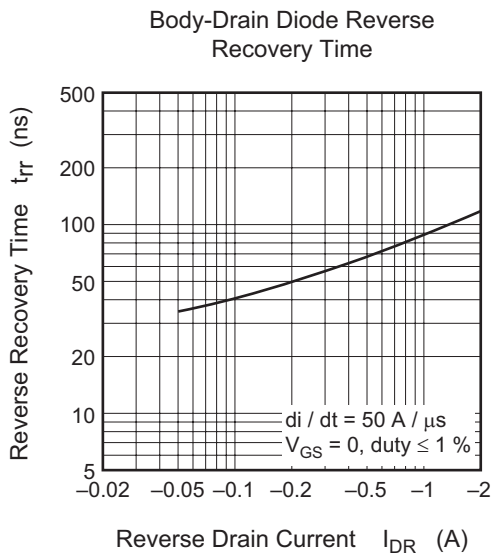
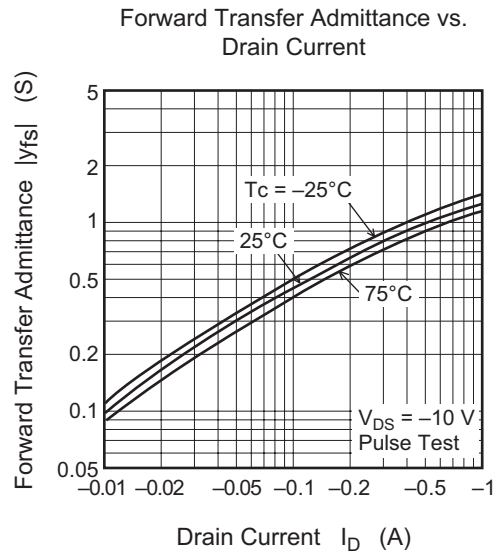
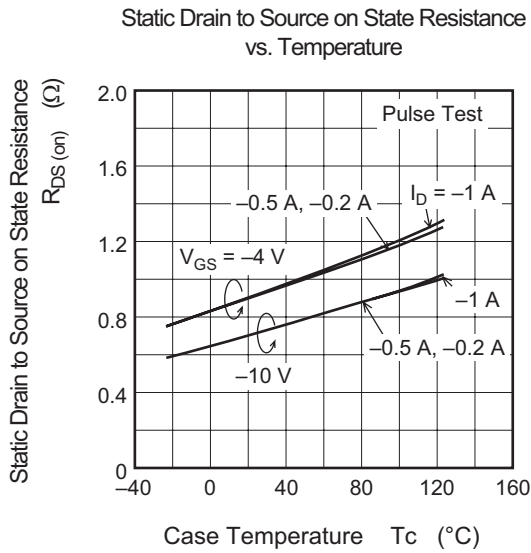
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-60	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±5	μA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-10	μA	V _{DS} = -50 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-1.0	—	-2.25	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.7	0.83	Ω	I _D = -0.5 A, V _{GS} = -10 V ^{Note 3}
	R _{DS (on)}	—	0.9	1.2	Ω	I _D = -0.5 A, V _{GS} = -4 V ^{Note 3}
Forward transfer admittance	y _{fs}	0.6	1.0	—	S	I _D = -0.5 A, V _{DS} = -10 V ^{Note 3}
Input capacitance	C _{iss}	—	160	—	pF	V _{DS} = -10 V V _{GS} = 0 f = 1 MHz
Output capacitance	C _{oss}	—	80	—	pF	
Reverse transfer capacitance	C _{rss}	—	28	—	pF	
Turn-on delay time	t _{d (on)}	—	7	—	ns	I _D = -0.5 A V _{GS} = -10 V R _L = 60 Ω
Rise time	t _r	—	8	—	ns	
Turn-off delay time	t _{d (off)}	—	30	—	ns	
Fall time	t _f	—	25	—	ns	
Body to drain diode forward voltage	V _{DF}	—	-1.1	—	V	I _F = -1 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	90	—	ns	I _F = -1 A, V _{GS} = 0 di _F /dt = 50 A/μs

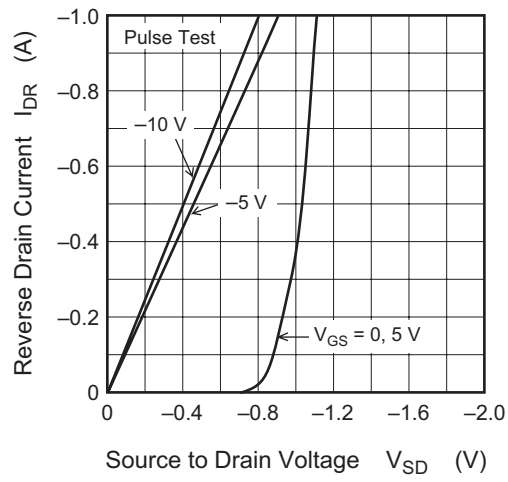
Note: 3. Pulse test

Main Characteristics

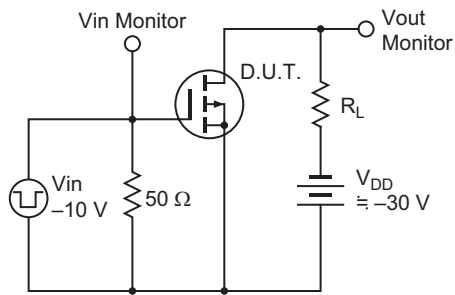




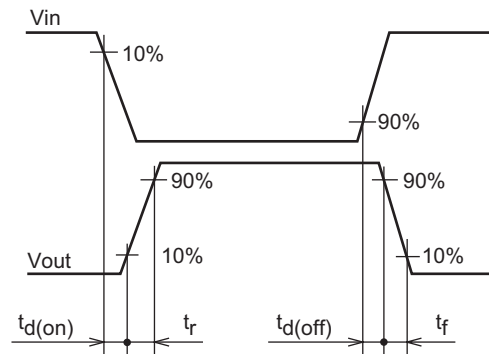
Reverse Drain Current vs. Source to Drain Voltage



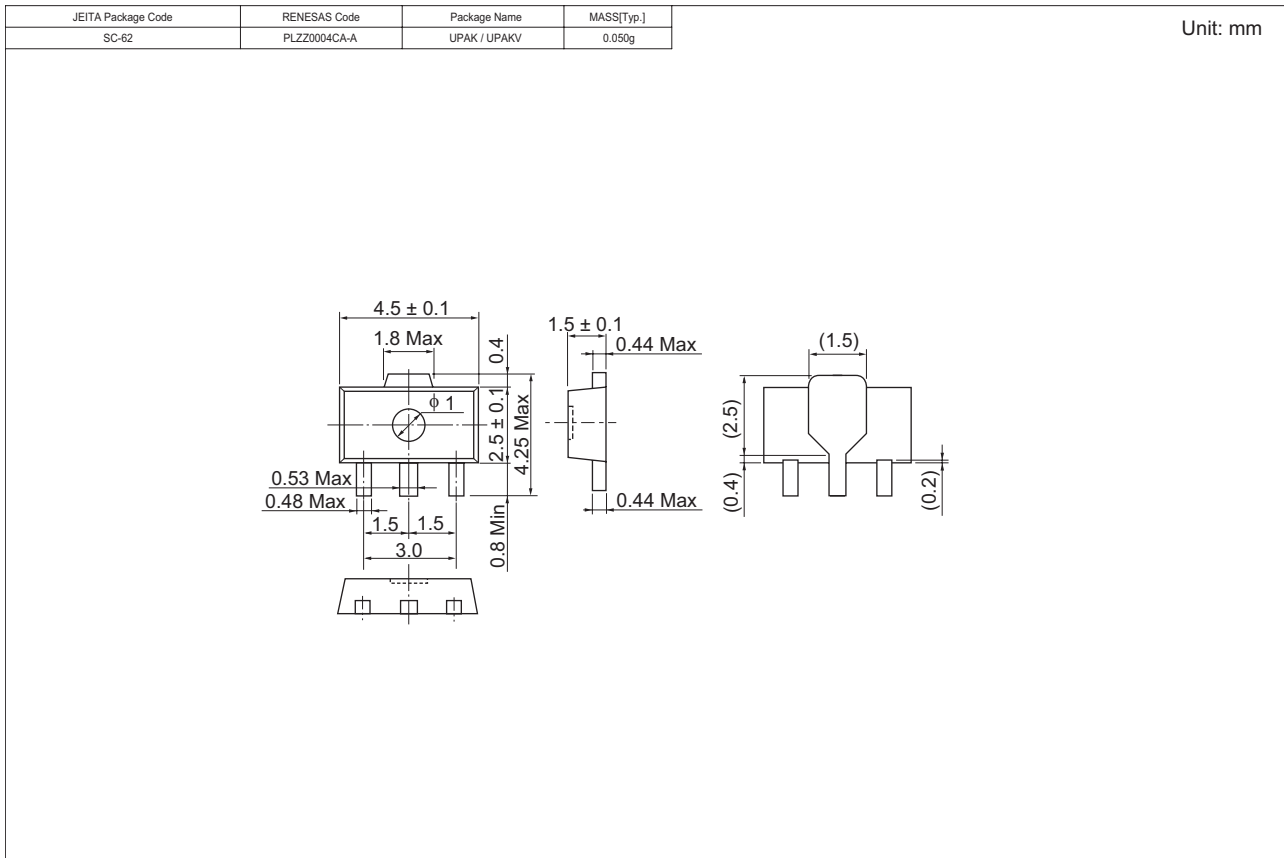
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SJ278MYTL-E	1000 pcs	Taping
2SJ278MYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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