Dual Low Offset, Low Power Operational Amplifier

OP200

FEATURES

Low input offset voltage: 75 µV maximum
Low offset voltage drift, over −55°C < T_A < +125°C
0.5 µV/°C maximum
Low supply current (per amplifier): 725 µA maximum
High open-loop gain: 5000 V/mV minimum
Low input bias current: 2 nA maximum
Low noise voltage density: 11 nV/√Hz at 1 kHz
Stable with large capacitive loads: 10 nF typical

PIN CONNECTIONS

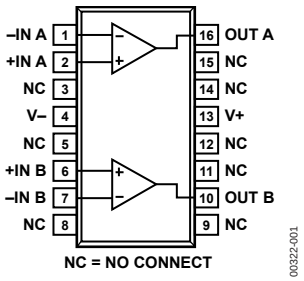


Figure 1. 16-Lead SOIC (S-Suffix)

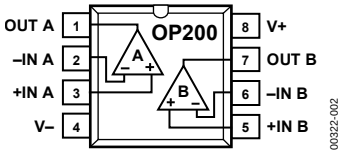


Figure 2. 8-Lead PDIP (P-Suffix)
8-Lead CERDIP (Z-Suffix)

GENERAL DESCRIPTION

The OP200 is the first monolithic dual operational amplifier to offer OP77 type precision performance. Available in the industry standard 8-lead pinout, the OP200 combines precision performance with the space and cost savings offered by a dual amplifier.

The OP200 features an extremely low input offset voltage of less than 75 µV with a drift below 0.5 µV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP200 exceeds 5,000,000 into a 10 kΩ load; input bias current is under 2 nA; CMRR is over 120 dB; and PSRR is below 1.8 µV/V. On-chip Zener zap trimming is used to achieve the extremely low input offset voltage of the OP200 and eliminates the need for offset pulling.

Power consumption of the OP200 is low, with each amplifier drawing less than 725 µA of supply current. The total current drawn by the dual OP200 is less than one-half that of a single OP07, yet the OP200 offers significant improvements over this industry-standard op amp. The voltage noise density of the OP200, 11 nV/√Hz at 1 kHz, is half that of most competitive devices.

The OP200 is pin compatible with the OP221, LM158, MC1458/MC1558, and LT1013.

The OP200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP400.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 1.

			OP200A/E			OP200G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS									
Input Offset Voltage	V_{OS}			25	75		80	200	µV
Long-Term Input Voltage Stability				0.1			0.1		µV/mo
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.05	1.0		0.05	3.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		0.1	2.0		0.1	5.0	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz		0.5			0.5		µV p-p
Input Noise Voltage Density[1]	e_n	f_O = 10 Hz		22	36		22		nV/√Hz
		f_O = 1000 Hz		11	18		11		nV/√Hz
Input Noise Current	i_n p-p	0.1 Hz to 10 Hz		15			15		pA p-p
Input Noise Current Density	i_n	f_O = 10 Hz		0.4			0.4		pA/√Hz
Input Resistance Differential Mode	R_{IN}			10			10		MΩ
Input Resistance Common Mode	R_{INCM}			125			125		GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V							
		R_L = 10 kΩ	5000	12000		3000	7000		M/mV
		R_L = 2 kΩ	2000	3700		1500	3200		M/mV

[1] Sample tested.

V_S = 15 V, −55°C ≤ T_A ≤ +125°C for OP200A, unless otherwise noted.

Table 2.

			OP200A			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			45	125	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	0.5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.15	2.5	nA
Input Bias Current	I_B	V_{CM} = 0 V		0.9	5.0	nA
Large Signal Voltage Gain	A_{VO}	V_O = 10 V				
		R_L = 10 Ω	3000	9000		V/mV
		R_L = 2 kΩ	1000	2700		V/mV
Input Voltage Range[1]	IVR		±12	±12.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	115	130		dB
Capacitive Load Stability		A_V = 1		8		nF
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 18 V		0.2	3.2	µV/V
Supply Current Per Amplifier	I_{SY}	No load		600	775	µA
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.4		V
		R_L = 2 kΩ	±11	±12		V

[1] Guaranteed by CMRR test.

V_S = ±15 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	OP200A/E			OP200G			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Input Voltage Range[1]	IVR		±12	±13		±12	±13		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	120	135		110	130		dB
Channel Separation[2]	CS	V_O = 20 V p-p, f_O = 10 Hz	123	145		123	145		dB
Input Capacitance	C_{IN}			3.2			3.2		pF
Capacitive Load Stability		A_V = 1, no oscillations		10			10		nF
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.4	1.8		0.6	5.6	µV/V
Supply Current Per Amplifier	I_{SY}	No load		570	725		570	725	µA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	V_O	R_L= 10 kΩ	±12	±12.6		±12	±12.6		V
		R_L = 2 kΩ	±11	±12.2		±11	±12.2		V
DYNAMIC PERFORMANCE									
Slew Rate	SR		0.1	0.15		0.1	0.15		V/µs
Gain Bandwidth Product	GBP	A_V = 1		500			500		kHz

[1] Guaranteed by CMRR test.
[2] Guaranteed but not 100% tested.

V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	OP200E			OP200G			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Input Offset Voltage	V_{OS}			35	100		110	300	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	0.5		0.6	2.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.08	2.5		0.1	6.0	nA
Input Bias Current	I_B	V_{CM} = 0 V		0 3	5.0		0.5	10.0	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V							
		R_L= 10 kΩ	3000	10,000		2000	5000		V/mV
		R_L = 2 kΩ	1500	3200		1000	2500		V/mV
Input Voltage Range[1]	IVR		±12	±12.5		±12	±12.5		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±12 V	115	130		105	130		dB
Capacitive Load Stability		A_V = 1, no oscillations		10			10		nF
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±18 V		0.15	3.2		0.3	10.0	µV/V
Supply Current Per Amplifier	I_{SY}	No load		600	775		600	775	µA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	V_O	R_L = 10 kΩ	±12	±12.4		±12	±12.4		V
		R_L = 2 kΩ	±11	±12		±11	±12.2		V

[1] Guaranteed by CMRR test.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	±20 V
Differential Input Voltage	±30 V
Input Voltage	Supply voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature Range (T_J)	−65°C to +150°C
Operating Temperature Range	
OP200A	−55°C to +125°C
OP200E, OP200G	−40°C to +85°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

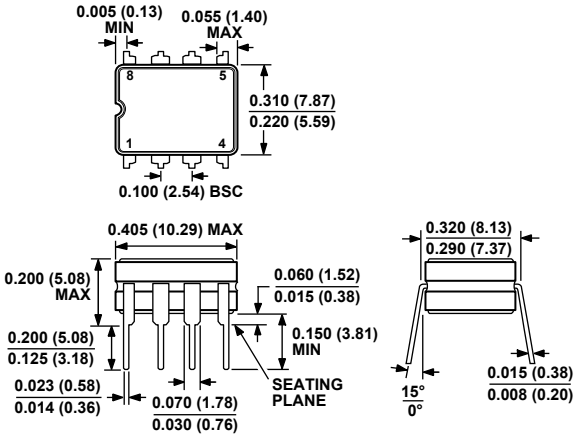
Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead CERDIP (Z Suffix)	148	16	°C/W
8-Lead Plastic DIP (P Suffix)	96	37	°C/W
16-Lead SOIC (S Suffix)	92	27	°C/W

[1] θ_{JA} is specified for worst-case mounting conditions, that is, θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 36. 8-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-8)
Z-Suffix
Dimensions shown in inches and (millimeters)

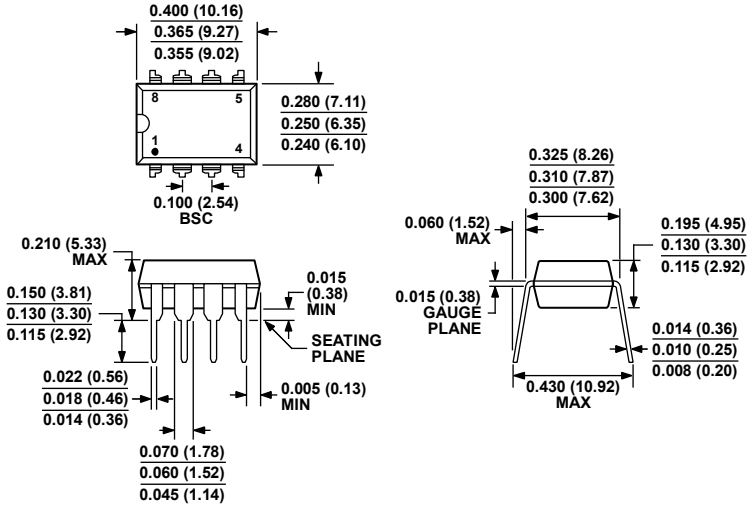


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Figure 37. 8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)
P-Suffix
Dimensions shown in inches and (millimeters)

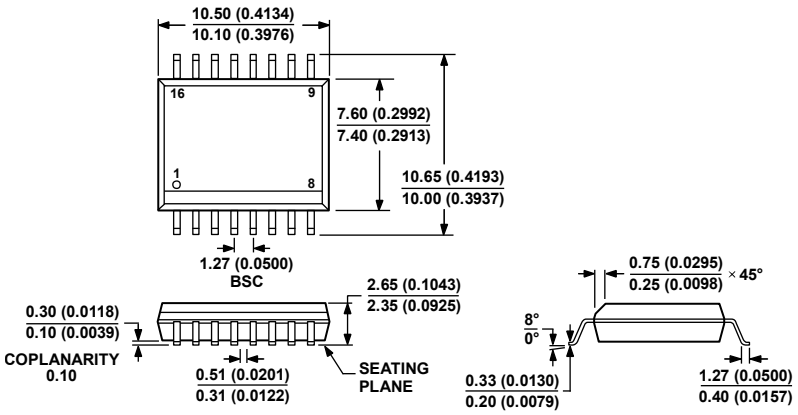

Figure 38. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
S-Suffix
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	T_A = 25°C V_{OS} Max (µV)	Temperature Range	Package Description	Package Option
OP200AZ[1]	75	−55°C to +125°C	8-Lead CERDIP	Z-Suffix (Q-8)
OP200EZ[1]	75	−40°C to +85°C	8-Lead CERDIP	Z-Suffix (Q-8)
OP200GP	200	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP200GPZ[1]	200	−40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
OP200GS	200	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP200GS-REEL	200	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP200GSZ[1]	200	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)
OP200GSZ-REEL[1]	200	−40°C to +85°C	16-Lead SOIC_W	S-Suffix (RW-16)

[1] Z = RoHS Compliant Part.