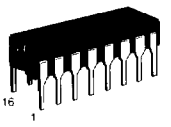
MOTOROLA

# MC14051B
# MC14052B
# MC14053B

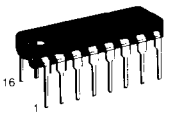
## ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally-controlled analog switches. The MC14051B effectively implements an SP8T solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range ($V_{DD} - V_{EE}$) = 3.0 to 18 V
  Note: $V_{EE}$ must be ≤ $V_{SS}$
- Linearized Transfer Characteristics
- Low-noise — 12 nV/√Cycle, f ≥ 1.0 kHz Typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower $R_{ON}$, Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices




**L SUFFIX**
CERAMIC
CASE 620




**P SUFFIX**
PLASTIC
CASE 648


**D SUFFIX**
SOIC
CASE 751B

**ORDERING INFORMATION**

| | |
|---|---|
| MC14XXXBCP | Plastic |
| MC14XXXBCL | Ceramic |
| MC14XXXBD | SOIC |

$T_A$ = −55° to 125°C for all packages.

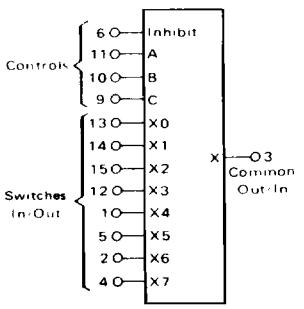
**MAXIMUM RATINGS***

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage (Referenced to $V_{EE}$. $V_{SS} \geq V_{EE}$) | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage (DC or Transient) (Referenced to $V_{SS}$ for Control Inputs and $V_{EE}$ for Switch I/O) | −0.5 to $V_{DD}$ +0.5 | V |
| $I_{in}$ | Input Current (DC or Transient), per Control Pin | ±10 | mA |
| $I_{sw}$ | Switch Through Current | ±25 | mA |
| $P_D$ | Power Dissipation, per Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8-Second Soldering) | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

**MC14051B**

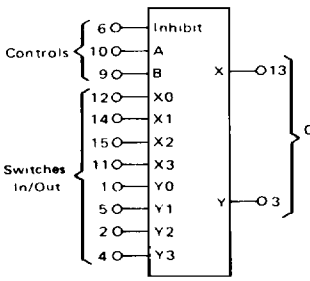
**8-Channel Analog Multiplexer/Demultiplexer**




$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8
$V_{EE}$ = Pin 7

**MC14052B**

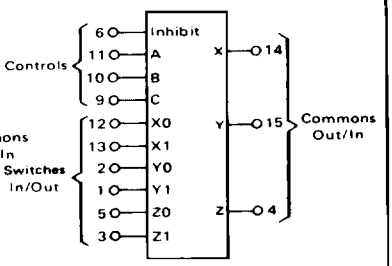
**Dual 4-Channel Analog Multiplexer/Demultiplexer**




$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8
$V_{EE}$ = Pin 7

**MC14053B**

**Triple 2-Channel Analog Multiplexer/Demultiplexer**




$V_{DD}$ = Pin 16
$V_{SS}$ = Pin 8
$V_{EE}$ = Pin 7

Note: Control Inputs referenced to $V_{SS}$. Analog Inputs and Outputs reference to $V_{EE}$. $V_{EE}$ must be ≤ $V_{SS}$.

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**ELECTRICAL CHARACTERISTICS**

| Characteristic | Symbol | $V_{DD}$ | Test Conditions | −55°C | | 25°C | | | 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Typ # | Max | Min | Max | |
| **SUPPLY REQUIREMENTS** (Voltages Referenced to $V_{EE}$) | | | | | | | | | | | |
| Power Supply Voltage Range | $V_{DD}$ | — | $V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$ | 3.0 | 18 | 3.0 | — | 18 | 3.0 | 18 | V |
| Quiescent Current Per Package | $I_{DD}$ | 5.0 | Control Inputs: | — | 5.0 | — | 0.005 | 5.0 | — | 150 | μA |
| | | 10 | $V_{in} = V_{SS}$ or $V_{DD}$, | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | 15 | Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and | — | 20 | — | 0.015 | 20 | — | 600 | |
| | | | $\Delta V_{switch} \leq 500$ mV** | | | | | | | | |
| Total Supply Current (Dynamic Plus Quiescent, Per Package | $I_{D(AV)}$ | 5.0 | $T_A = 25°C$ only (The channel component, $(V_{in} - V_{out})/R_{on}$ is not included.) | Typical | | | (0.07 μA/kHz)f + $I_{DD}$ | | | | μA |
| | | 10 | | | | | (0.20 μA/kHz)f + $I_{DD}$ | | | | |
| | | 15 | | | | | (0.36 μA/kHz)f + $I_{DD}$ | | | | |
| **CONTROL INPUTS — INHIBIT, A, B, C** (Voltages Referenced to $V_{SS}$) | | | | | | | | | | | |
| Low-Level Input Voltage | $V_{IL}$ | 5.0 | $R_{on}$ = per spec. | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | V |
| | | 10 | $I_{off}$ = per spec | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| | | 15 | | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| High-Level Input Voltage | $V_{IH}$ | 5.0 | $R_{on}$ = per spec. | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | V |
| | | 10 | $I_{off}$ = per spec | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | 15 | | 11 | — | 11 | 8.25 | — | 11 | — | |
| Input Leakage Current | $I_{in}$ | 15 | $V_{in} = 0$ or $V_{DD}$ | — | ±0.1 | — | +0.00001 | ±0.1 | — | ±1.0 | μA |
| Input Capacitance | $C_{in}$ | — | | — | — | — | 5.0 | 7.5 | — | — | pF |
| **SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z** (Voltages Referenced to $V_{EE}$) | | | | | | | | | | | |
| Recommended Peak-to-Peak Voltage Into or Out of the Switch | $V_{I/O}$ | — | Channel On or Off | 0 | $V_{DD}$ | 0 | — | $V_{DD}$ | 0 | $V_{DD}$ | $V_{PP}$ |
| Recommended Static or Dynamic Voltage Across the Switch** (Figure 5) | $\Delta V_{switch}$ | — | Channel On | 0 | 600 | 0 | — | 600 | 0 | 300 | mV |
| Output Offset Voltage | $V_{OO}$ | — | $V_{in} = 0$ V, No Load | — | — | — | 10 | — | — | — | μV |
| ON Resistance | $R_{on}$ | 5.0 | $\Delta V_{switch} \leq 500$ mV**, | — | 800 | — | 250 | 1050 | — | 1200 | Ω |
| | | 10 | $V_{in} = V_{IL}$ or $V_{IH}$ | — | 400 | — | 120 | 500 | — | 520 | |
| | | 15 | (Control), and $V_{in}$ = 0 to $V_{DD}$ (Switch) | — | 220 | — | 80 | 280 | — | 300 | |
| ΔON Resistance Between Any Two Channels in the Same Package | $\Delta R_{on}$ | 5.0 | | — | 70 | — | 25 | 70 | — | 135 | Ω |
| | | 10 | | — | 50 | — | 10 | 50 | — | 95 | |
| | | 15 | | — | 45 | — | 10 | 45 | — | 65 | |
| Off-Channel Leakage Current (Figure 10) | $I_{off}$ | 15 | $V_{in} = V_{IL}$ or $V_{IH}$ (Control) Channel to Channel or Any One Channel | — | ±100 | — | ±0.05 | ±100 | — | ±1000 | nA |
| Capacitance, Switch I/O | $C_{I/O}$ | — | Inhibit = $V_{DD}$ | — | — | — | 10 | — | — | — | pF |
| Capacitance, Common O/I | $C_{O/I}$ | — | Inhibit = $V_{DD}$ | | | | | | | | pF |
| | | | (MC14051B) | — | — | — | 60 | — | — | — | |
| | | | (MC14052B) | — | — | — | 32 | — | — | — | |
| | | | (MC14053B) | — | — | — | 17 | — | — | — | |
| Capacitance, Feedthrough (Channel Off) | $C_{I/O}$ | — | Pins Not Adjacent | — | — | — | 0.15 | — | — | — | pF |
| | | — | Pins Adjacent | — | — | — | 0.47 | — | — | — | |

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
**For voltage drops across the switch ($\Delta V_{switch}$) >600 mV (>300 mV at high temperature), excessive $V_{DD}$ current may be drawn; i.e. the current out of the switch may contain both $V_{DD}$ and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

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**ELECTRICAL CHARACTERISTICS* ($C_L$ = 50 pF, $T_A$ = 25°C) ($V_{EE} \leq V_{SS}$ unless otherwise indicated)**

| Characteristic | Symbol | $V_{DD}$-$V_{EE}$ Vdc | Typ # All Types | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times (Figure 6) | $t_{PLH}$, $t_{PHL}$ | | | | ns |
| Switch Input to Switch Output ($R_L$ = 10 kΩ) | | | | | |
| MC14051 | | | | | |
| $t_{PLH}$, $t_{PHL}$ = (0.17 ns/pF) $C_L$ + 26.5 ns | | 5.0 | 35 | 90 | |
| $t_{PLH}$, $t_{PHL}$ = (0.08 ns/pF) $C_L$ + 11 ns | | 10 | 15 | 40 | |
| $t_{PLH}$, $t_{PHL}$ = (0.06 ns/pF) $C_L$ + 9.0 ns | | 15 | 12 | 30 | |
| MC14052 | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.17 ns/pF) $C_L$ + 21.5 ns | | 5.0 | 30 | 75 | |
| $t_{PLH}$, $t_{PHL}$ = (0.08 ns/pF) $C_L$ + 8.0 ns | | 10 | 12 | 30 | |
| $t_{PLH}$, $t_{PHL}$ = (0.06 ns/pF) $C_L$ + 7.0 ns | | 15 | 10 | 25 | |
| MC14053 | | | | | ns |
| $t_{PLH}$, $t_{PHL}$ = (0.17 ns/pF) $C_L$ + 16.5 ns | | 5.0 | 25 | 65 | |
| $t_{PLH}$, $t_{PHL}$ = (0.08 ns/pF) $C_L$ + 4.0 ns | | 10 | 8.0 | 20 | |
| $t_{PLH}$, $t_{PHL}$ = (0.06 ns/pF) $C_L$ + 3.0 ns | | 15 | 6.0 | 15 | |
| Inhibit to Output ($R_L$ = 10 kΩ, $V_{EE}$ = $V_{SS}$) Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level | $t_{PHZ}$, $t_{PLZ}$, $t_{PZH}$, $t_{PZL}$ | | | | ns |
| MC14051B | | 5.0 | 350 | 700 | |
| | | 10 | 170 | 340 | |
| | | 15 | 140 | 280 | |
| MC14052B | | 5.0 | 300 | 600 | ns |
| | | 10 | 155 | 310 | |
| | | 15 | 125 | 250 | |
| MC14053B | | 5.0 | 275 | 550 | ns |
| | | 10 | 140 | 280 | |
| | | 15 | 110 | 220 | |
| Control Input to Output ($R_L$ = 10 kΩ, $V_{EE}$ = $V_{SS}$) | $t_{PLH}$, $t_{PHL}$ | | | | ns |
| MC14051B | | 5.0 | 360 | 720 | |
| | | 10 | 160 | 320 | |
| | | 15 | 120 | 240 | |
| MC14052B | | 5.0 | 325 | 650 | ns |
| | | 10 | 130 | 260 | |
| | | 15 | 90 | 180 | |
| MC14053B | | 5.0 | 300 | 600 | ns |
| | | 10 | 120 | 240 | |
| | | 15 | 80 | 160 | |
| Second Harmonic Distortion ($R_L$ = 10KΩ, f = 1kHz) $V_{in}$ = 5 $V_{PP}$ | – | 10 | 0.07 | – | % |
| Bandwidth (Figure 7) ($R_L$ = 1 kΩ, $V_{in}$ = 1/2 ($V_{DD}$-$V_{EE}$) p-p, $C_L$ = 50pF 20 Log $\frac{V_{out}}{V_{in}}$ = - 3 dB) | BW | 10 | 17 | — | MHz |
| Off Channel Feedthrough Attenuation (Figure 7) $R_L$ = 1KΩ, $V_{in}$ = 1/2 ($V_{DD}$ - $V_{EE}$) p-p | – | 10 | −50 | — | dB |
| $f_{in}$ = 4.5 MHz — MC14051B | | | | | |
| $f_{in}$ = 30 MHz — MC14052B | | | | | |
| $f_{in}$ = 55 MHz — MC14053B | | | | | |
| Channel Separation (Figure 8) ($R_L$ = 1 kΩ, $V_{in}$ = 1/2 ($V_{DD}$-$V_{EE}$) p-p, $f_{in}$ = 3.0 MHz | – | 10 | −50 | – | dB |
| Crosstalk, Control Input to Common O/I (Figure 9) ($R_1$ = 1 kΩ, $R_L$ = 10 kΩ Control $t_{TLH}$ = $t_{THL}$ = 20 ns, Inhibit = $V_{SS}$) | – | 10 | 75 | – | mV |

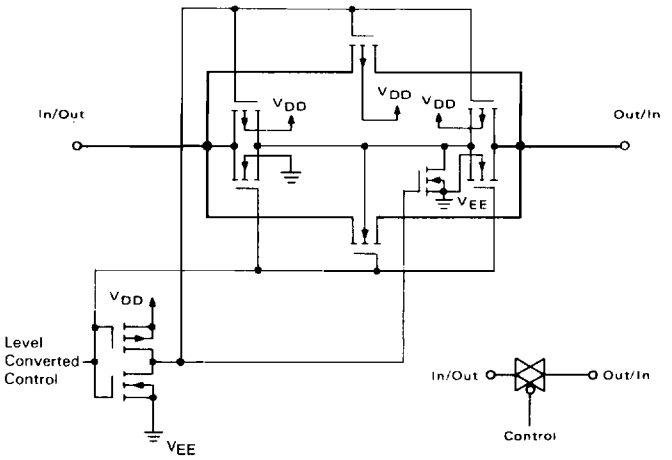
*The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$, $V_{EE}$, or $V_{DD}$). Unused outputs must be left open.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC




TRUTH TABLE

| Control Inputs | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Select | | | ON Switches | | | | |
| Inhibit | C* | B | A | MC14051B | MC14052B | | MC14053B | |
| 0 | 0 | 0 | 0 | X0 | Y0 | X0 | Z0 | Y0 X0 |
| 0 | 0 | 0 | 1 | X1 | Y1 | X1 | Z0 | Y0 X1 |
| 0 | 0 | 1 | 0 | X2 | Y2 | X2 | Z0 | Y1 X0 |
| 0 | 0 | 1 | 1 | X3 | Y3 | X3 | Z0 | Y1 X1 |
| 0 | 1 | 0 | 0 | X4 | | | Z1 | Y0 X0 |
| 0 | 1 | 0 | 1 | X5 | | | Z1 | Y0 X1 |
| 0 | 1 | 1 | 0 | X6 | | | Z1 | Y1 X0 |
| 0 | 1 | 1 | 1 | X7 | | | Z1 | Y1 X1 |
| 1 | x | x | x | None | None | | None | |

*Not applicable for MC14052
x = Don't Care

FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM

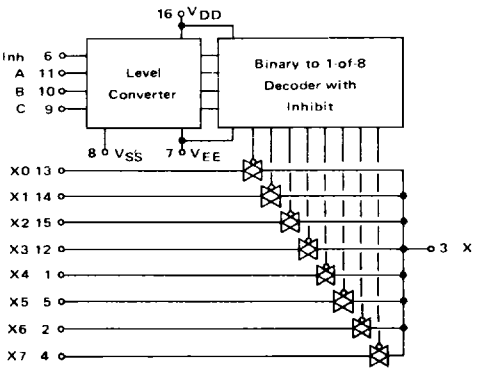



FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

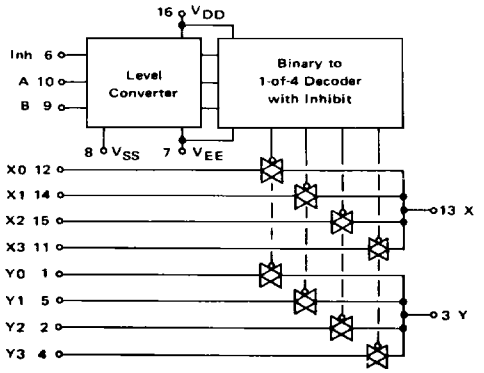
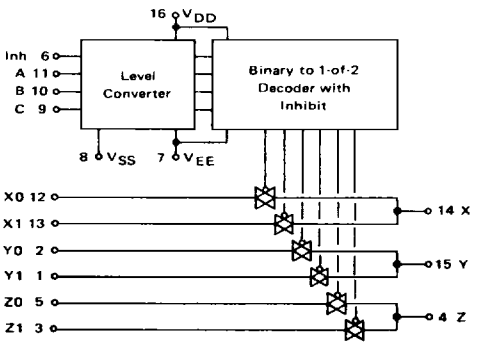



FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM



## TEST CIRCUITS

FIGURE 5 — ΔV ACROSS SWITCH

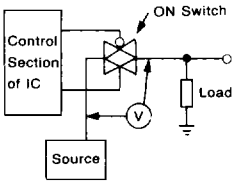



FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

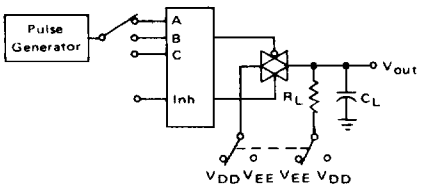



FIGURE 7 — BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

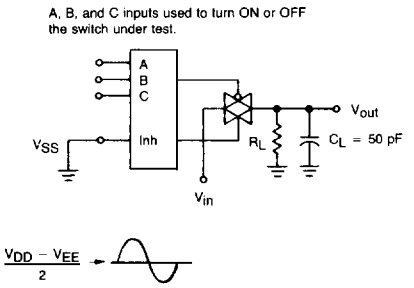



FIGURE 8 — CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

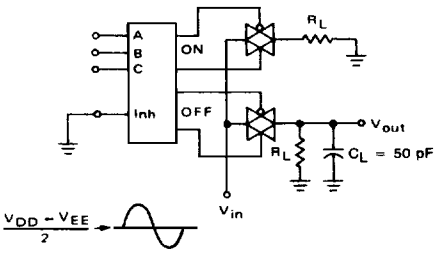



FIGURE 9 — CROSSTALK, CONTROL INPUT TO COMMON O/I

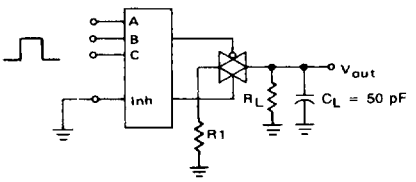
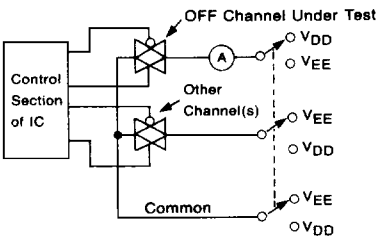



FIGURE 10 — OFF CHANNEL LEAKAGE




NOTE: See also Figures 7 and 8 on Page 6-51.

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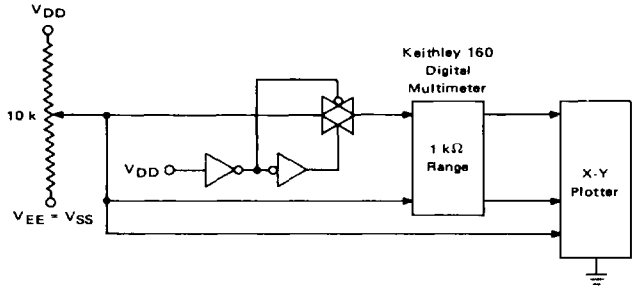
FIGURE 11 – CHANNEL RESISTANCE ($R_{ON}$) TEST CIRCUIT




## TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – $V_{DD}$ = 7.5 V, $V_{EE}$ = -7.5 V

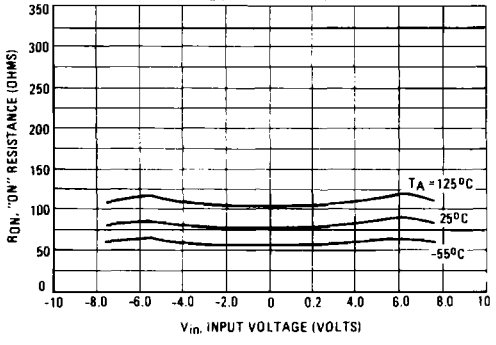



FIGURE 13 – $V_{DD}$ = 5.0 V, $V_{EE}$ = -5.0 V

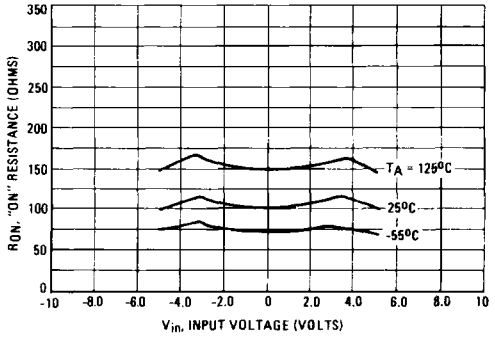



FIGURE 14 – $V_{DD}$ = 2.5 V, $V_{EE}$ = -2.5 V

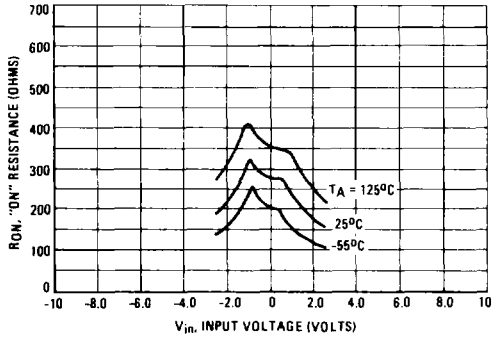
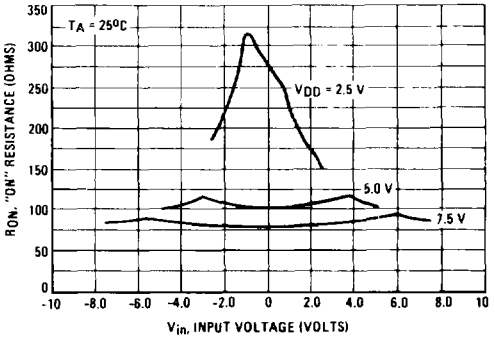



FIGURE 15 – COMPARISON AT 25°C, $V_{DD}$ = -$V_{EE}$

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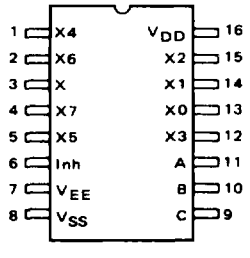
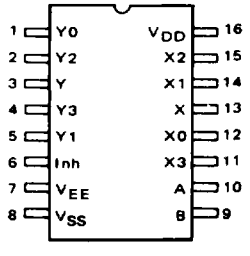
PIN ASSIGNMENT

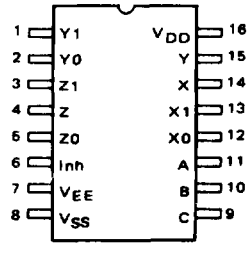
MC14051B




MC14052B




MC14053B



## APPLICATIONS INFORMATION

Figure A illustrates use of the on-chip level converter detailed in Figures 2, 3, and 4. The 0-to-5 V Digital Control signal is used to directly control a 9 $V_{p-p}$ analog signal.

The digital control logic levels are determined by $V_{DD}$ and $V_{SS}$. The $V_{DD}$ voltage is the logic high voltage; the $V_{SS}$ voltage is logic low. For the example, $V_{DD}$ = +5 V = logic high at the control inputs; $V_{SS}$ = GND = 0 V = logic low.

The maximum analog signal level is determined by $V_{DD}$ and $V_{EE}$. The $V_{DD}$ voltage determines the maximum recommended peak above $V_{SS}$. The $V_{EE}$ voltage determines the maximum swing below $V_{SS}$. For the example, $V_{DD} - V_{SS}$ = 5 V maximum swing above $V_{SS}$; $V_{SS} - V_{EE}$ = 5 V maximum swing below $V_{SS}$. The example shows a ± 4.5 V signal which allows a ½ volt margin at each peak. If voltage transients above $V_{DD}$ and/or below $V_{EE}$ are anticipated on the analog channels, external diodes ($D_X$) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between $V_{DD}$ and $V_{EE}$ is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between $V_{DD}$ and $V_{EE}$.

Balanced supplies are not required. However, $V_{SS}$ must be greater than or equal to $V_{EE}$. For example, $V_{DD}$ = +10 V, $V_{SS}$ = +5 V, and $V_{EE}$ = −3 V is acceptable. See the Table below.

FIGURE A — APPLICATION EXAMPLE

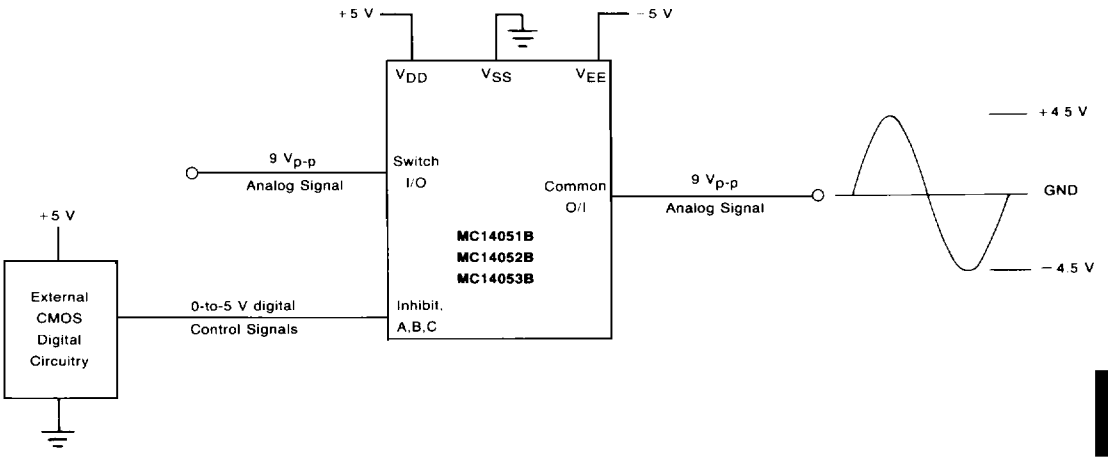
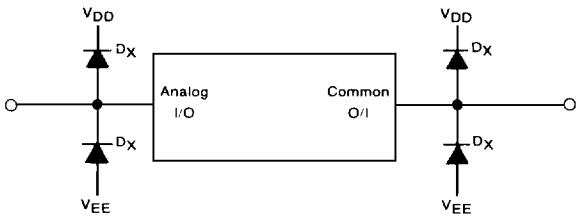



FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES




### POSSIBLE SUPPLY CONNECTIONS

| $V_{DD}$ In Volts | $V_{SS}$ In Volts | $V_{EE}$ In Volts | Control Inputs Logic High/Logic Low In Volts | Maximum Analog Signal Range In Volts |
|---|---|---|---|---|
| +8 | 0 | −8 | +8/0 | +8 to −8 = 16 $V_{p-p}$ |
| +5 | 0 | −12 | +5/0 | +5 to −12 = 17 $V_{p-p}$ |
| +5 | 0 | 0 | +5/0 | +5 to 0 = 5 $V_{p-p}$ |
| +5 | 0 | −5 | +5/0 | +5 to −5 = 10 $V_{p-p}$ |
| +10 | +5 | −5 | +10/+5 | +10 to −5 = 15 $V_{p-p}$ |