HM628128D Series

1 M SRAM (128-kword × 8-bit)

HITACHI

ADE-203-996 (Z)
Preliminary, Rev. 0.0
Jan. 20, 1999

Description

The Hitachi HM628128D Series is 1-Mbit static RAM organized 131,072-kword × 8-bit. HM628128D Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. The HM628128D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has package variations of standard 32-pin plastic DIP, standard 32-pin plastic SOP and standard 32-pin plastic TSOPI.

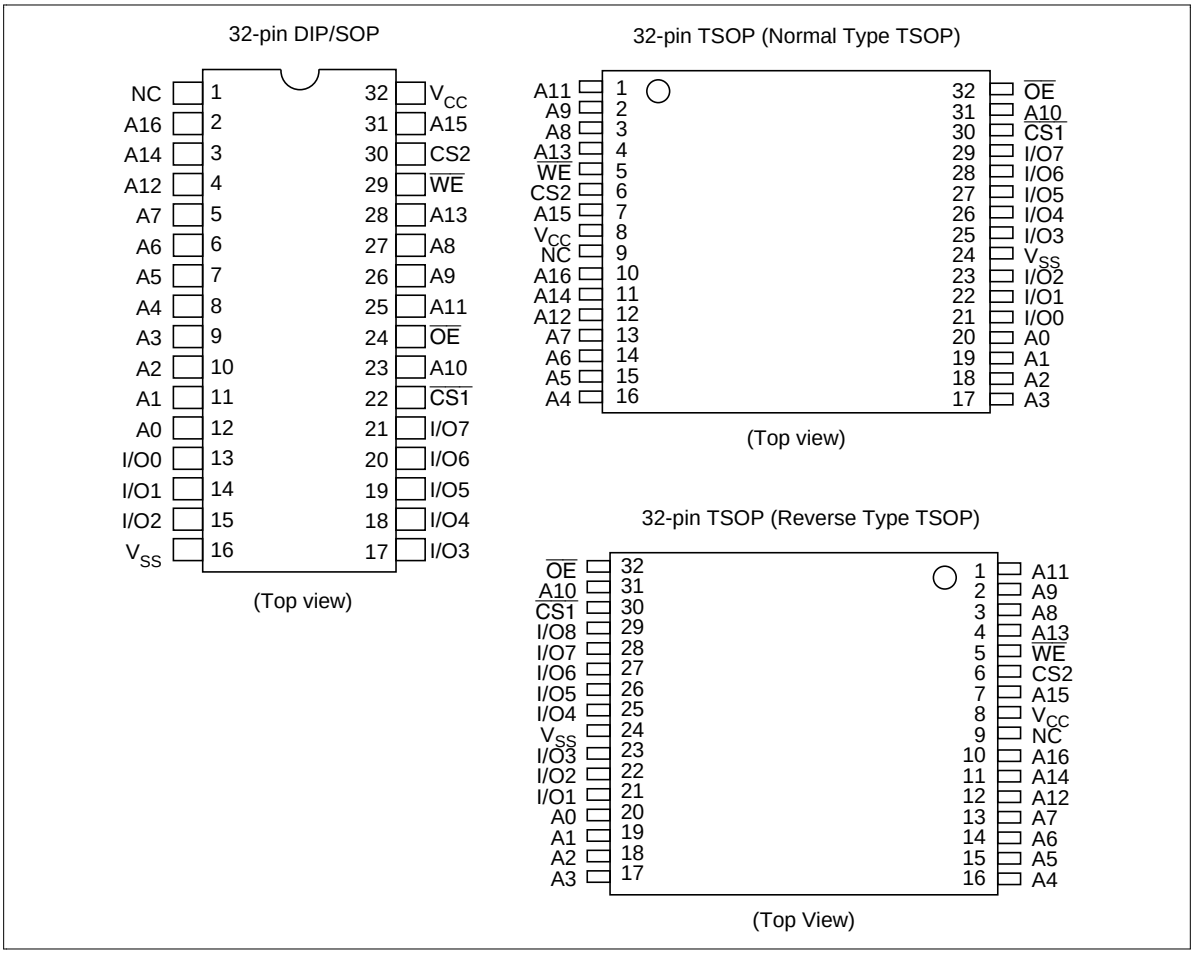
Features

- Single 5 V supply: 5 V ± 10%
- Access time: 55 ns/70 ns (max)
- Power dissipation
  - Active: 30 mW/MHz (typ)
  - Standby: 10 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible all inputs
- Battery backup operation
  - 2 chip selection for battery backup

Ordering Information

Type No.	Access time	Package
HM628128DLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628128DLP-7	70 ns	
HM628128DLP-5SL	55 ns	
HM628128DLP-7SL	70 ns	
HM628128DLP-5UL	55 ns	
HM628128DLP-7UL	70 ns	
HM628128DLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628128DLFP-7	70 ns	
HM628128DLFP-5SL	55 ns	
HM628128DLFP-7SL	70 ns	
HM628128DLFP-5UL	55 ns	
HM628128DLFP-7UL	70 ns	
HM628128DLTS-5	55 ns	8 × 13.4 mm 32-pin plastic TSOP I (TFP-32DC)
HM628128DLTS-7	70 ns	
HM628128DLTS-5SL	55 ns	
HM628128DLTS-7SL	70 ns	
HM628128DLTS-5UL	55 ns	
HM628128DLTS-7UL	70 ns	
HM628128DLT-5	55 ns	Normal-bend type 8 × 20 mm 32-pin plastic TSOP I (TFP-32D)
HM628128DLT-7	70 ns	
HM628128DLT-5SL	55 ns	
HM628128DLT-7SL	70 ns	
HM628128DLT-5UL	55 ns	
HM628128DLT-7UL	70 ns	
HM628128DLR-5	55 ns	Reverse-bend type 8 × 20 mm 32-pin plastic TSOP I (TFP-32DR)
HM628128DLR-7	70 ns	
HM628128DLR-5SL	55 ns	
HM628128DLR-7SL	70 ns	
HM628128DLR-5UL	55 ns	
HM628128DLR-7UL	70 ns	

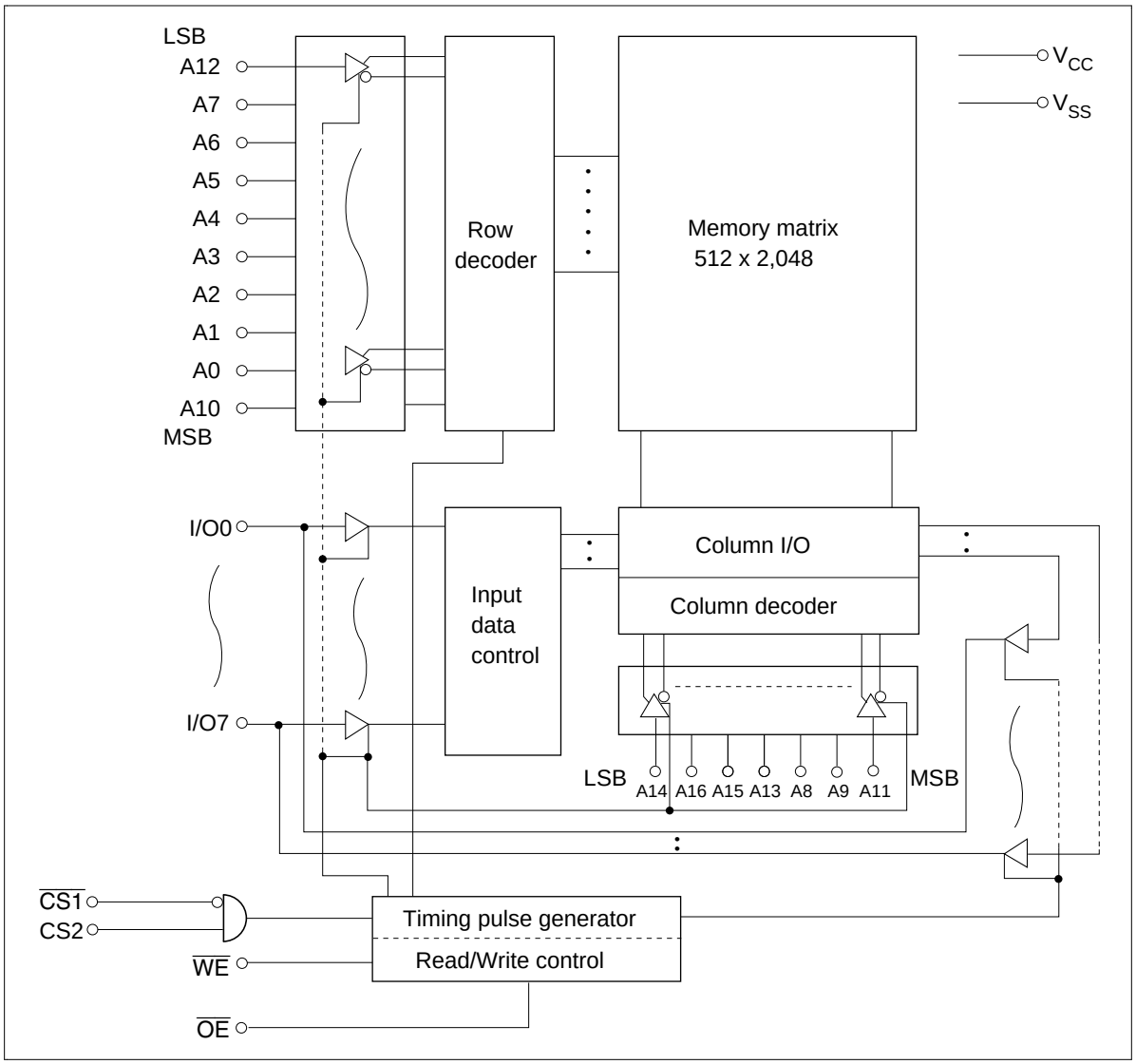
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	I/O	Operation
H	H	×	×	High-Z	Standby
L	L	×	×	High-Z	Standby
L	L	×	×	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	H	Din	Write
L	H	L	L	Din	Write
L	H	H	H	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–20 to +85	°C

Notes: 1. V_T min: –1.5 V for pulse half-width ≤ 30 ns
2. Maximum voltage is +7.0 V

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	0.8	V	1
Ambient temperature range	Ta	–20	—	+70	°C	

Note: 1. V_{IL} min: –1.5 V for pulse half-width ≤ 30 ns

DC Characteristics

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	15	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	60	mA	Min cycle, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	6	20	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current	I_{SB}	—	—	2	mA	(1) $\overline{CS1}$ = V_{IH}, CS2 = V_{IH}, or (2) CS2 = V_{IL}
	I_{SB1}*[2]	—	2	100	µA	0 V ≤ Vin (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1}$ ≥ V_{CC} – 0.2 V, CS2 ≥ V_{CC} – 0.2 V
	I_{SB1}*[3]	—	2	50	µA	
	I_{SB1}*[4]	—	1	20	µA	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.
4. This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –20 to +70°C, V_{CC} = 5.0 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.8 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.5 V
- Output timing reference level: 1.5 V
- Output load: 1 TTL Gate+ CL (100 pF) (HM628128D-7)
  1 TTL Gate+ CL (50 pF) (HM628128D-5)
  (Including scope and jig)

Read Cycle

		HM628128D					
		-5		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	55	—	70	—	ns	
Address access time	t_{AA}	—	55	—	70	ns	
Chip select access time	t_{ACS1}	—	55	—	70	ns	
	t_{ACS2}	—	55	—	70	ns	
Output enable to output valid	t_{OE}	—	30	—	35	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
Chip selection to output in low-Z	t_{CLZ1}	10	—	10	—	ns	2, 3
	t_{CLZ2}	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1, 2, 3
	t_{CHZ2}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 3

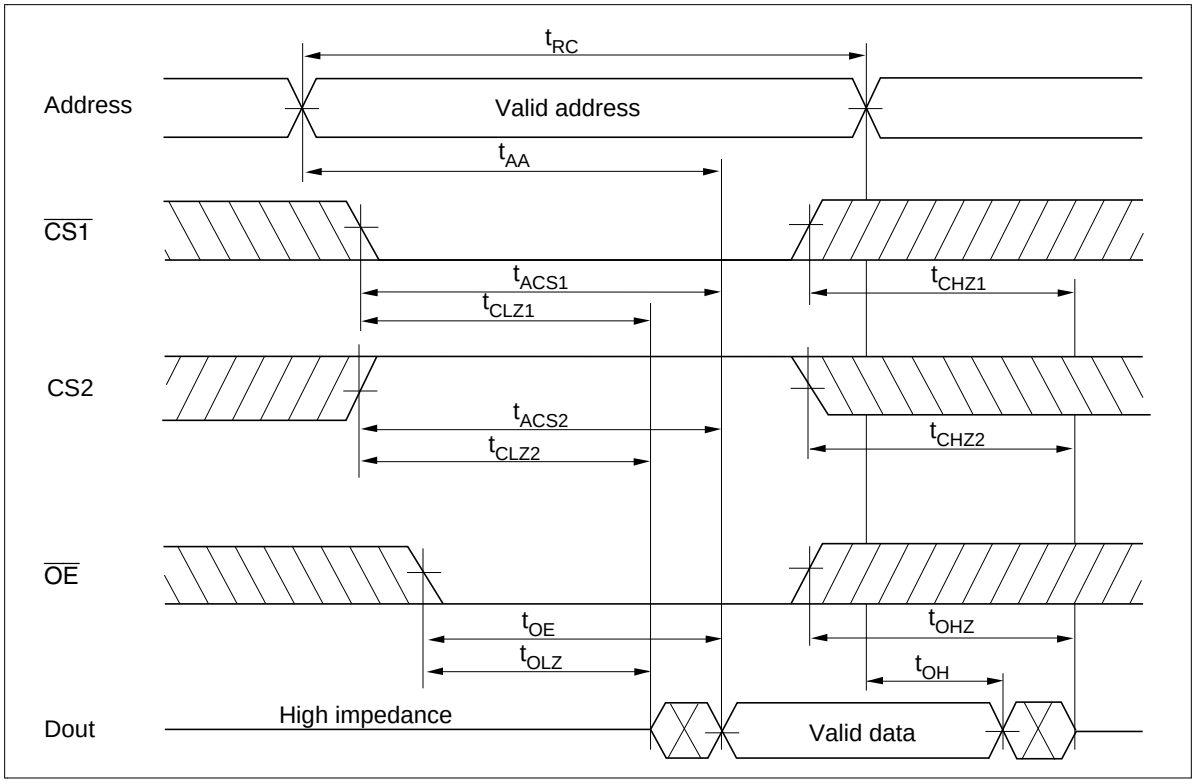
Write Cycle

		HM628128D					
		-5		-7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	55	—	70	—	ns	
Address valid to end of write	t_{AW}	50	—	60	—	ns	
Chip selection to end of write	t_{CW}	50	—	60	—	ns	5
Write pulse width	t_{WP}	40	—	50	—	ns	4, 13
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	20	—	25	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1, 2, 8
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	20	0	25	ns	1, 2, 8

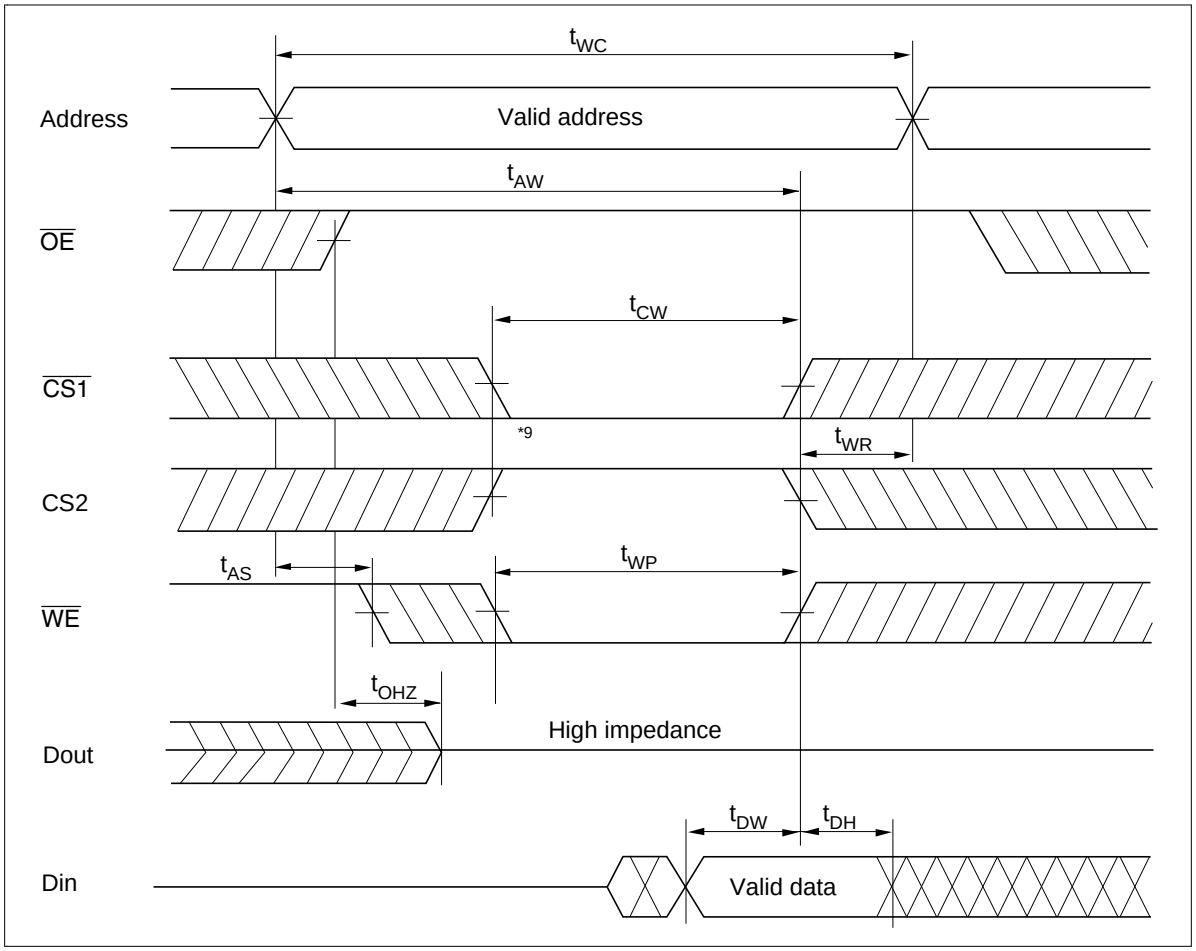
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS1}$ going low, CS2 going high, or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS1}$ going high, CS2 going low, or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS1}$ going high or CS2 going low to the end of write cycle.
8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
9. If the $\overline{CS1}$ goes low or CS2 going high simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the output remain in a high impedance state.
10. Dout is the same phase of the write data of this write cycle.
11. Dout is the read data of next address.
12. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
13. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveforms

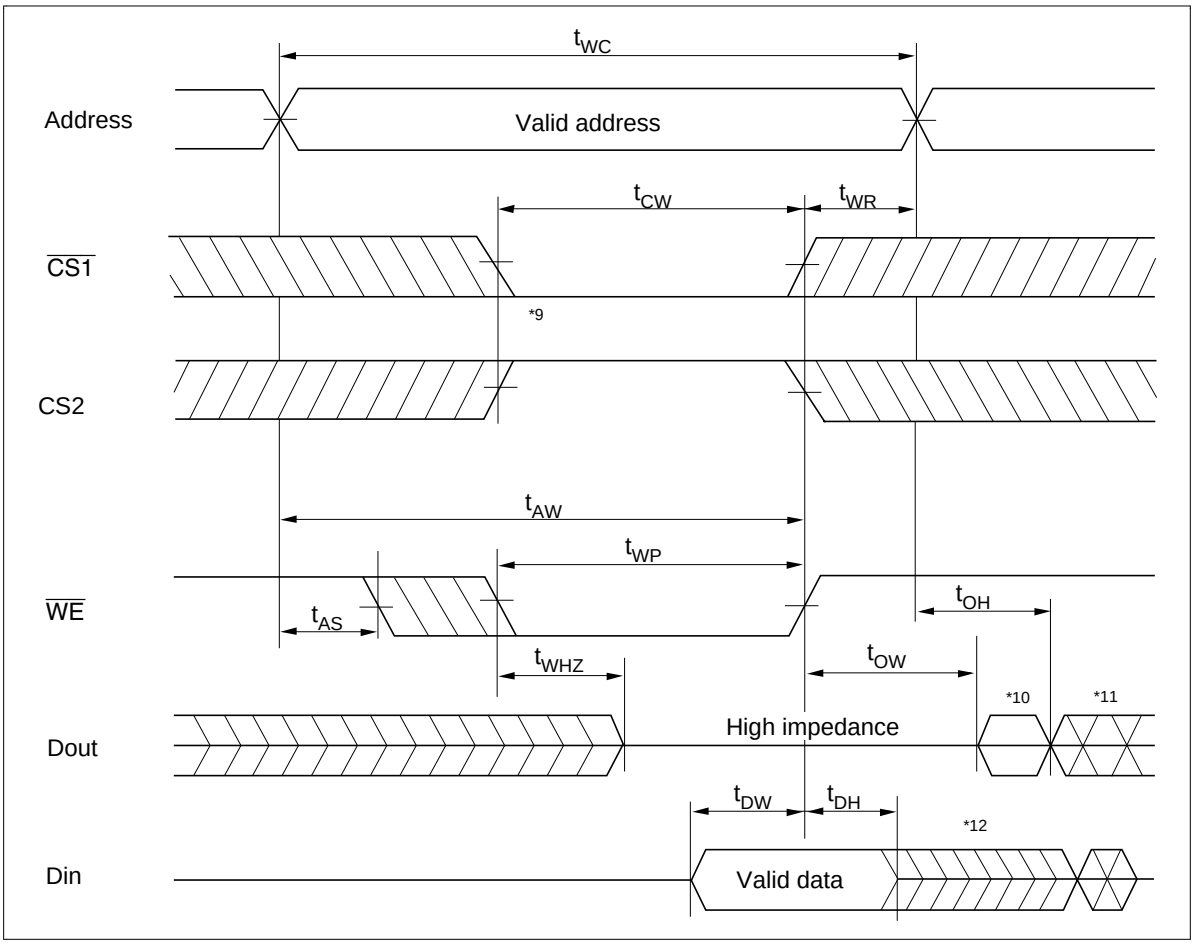
Read Cycle ($\overline{WE}$ = V_{IH})



Write Cycle (1) ($\overline{OE}$ Clock)



Write Cycle (2) ($\overline{OE}$ = V_{IL})

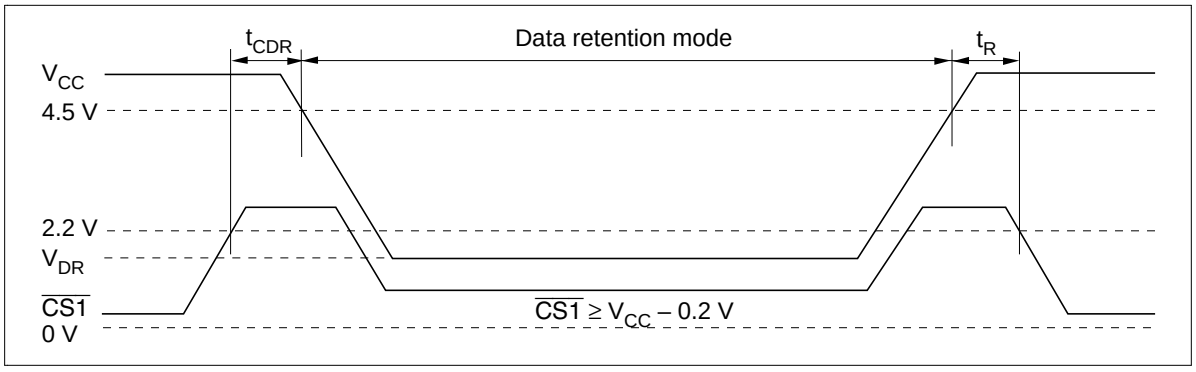


Low V_{CC} Data Retention Characteristics (Ta = –20 to +70°C)

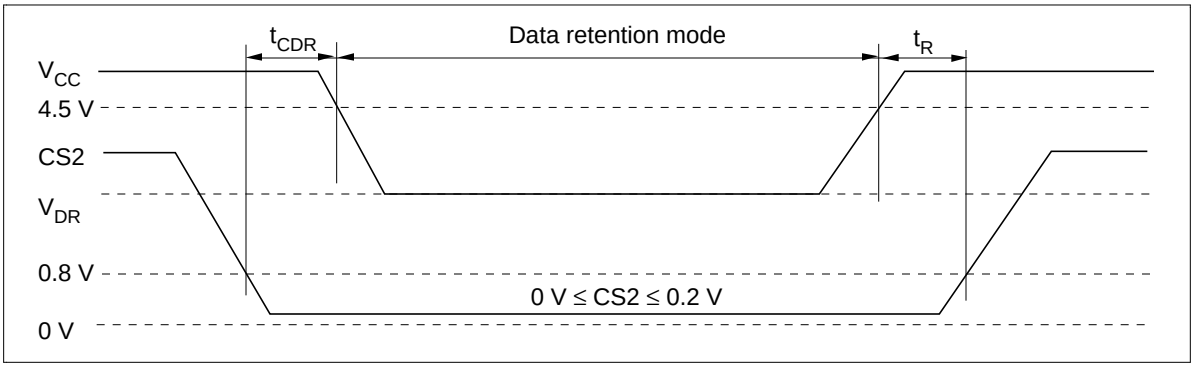
Parameter	Symbol	Min	Typ*5	Max	Unit	Test conditions*4
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Data retention current	I_{CCDR}*1	—	1.0	50	µA	V_{CC} = 3.0 V, Vin ≥ 0 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V
	I_{CCDR}*2	—	1.0	15	µA	
	I_{CCDR}*3	—	0.5	10	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*6	—	—	ns	

Notes: 1. This characteristic is guaranteed only for L-version, 20 µA max. at Ta = –20 to +40°C.
2. This characteristic is guaranteed only for L-SL-version, 3 µA max. at Ta = –20 to +40°C.
3. This characteristic is guaranteed only for L-UL-version, 1 µA max. at Ta = –20 to +40°C.
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{CC} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
5. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
6. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



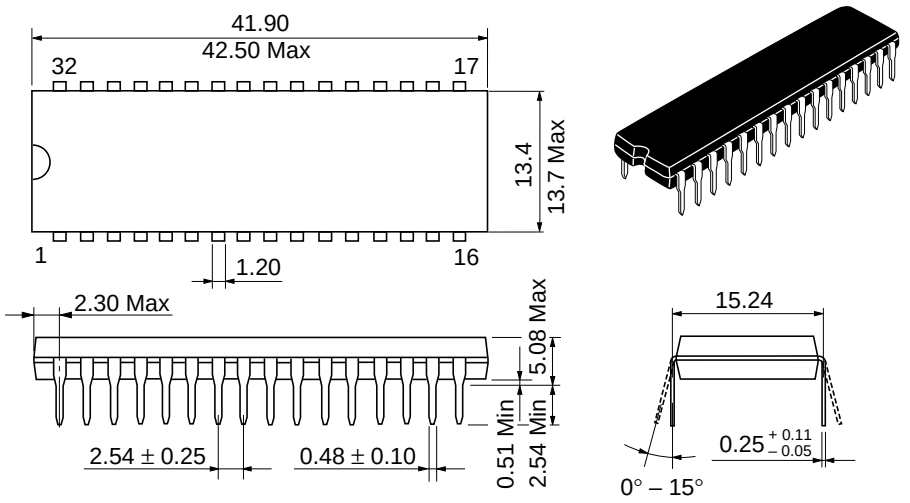
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM628128DLP Series (DP-32)

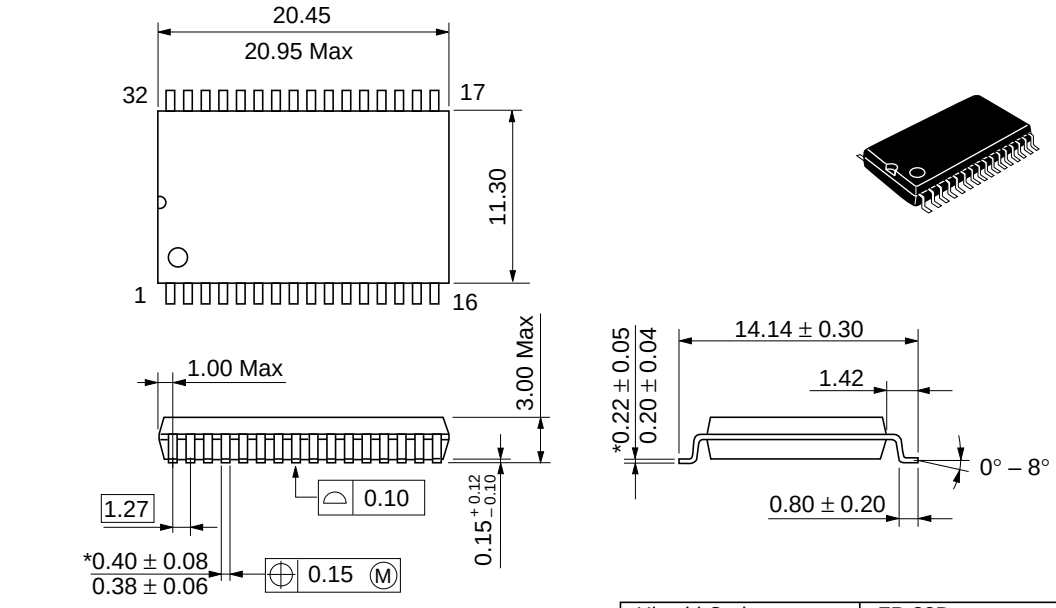
Unit: mm



Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

HM628128DLFP Series (FP-32D)

Unit: mm

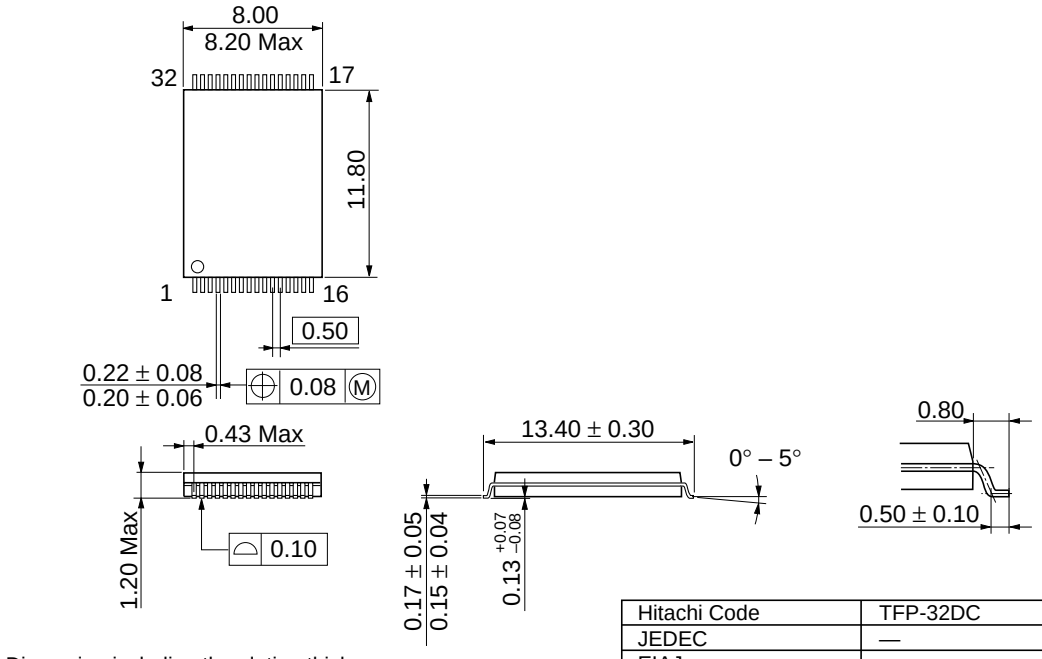


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

HM628128DLTS Series (TFP-32DC)

Unit: mm

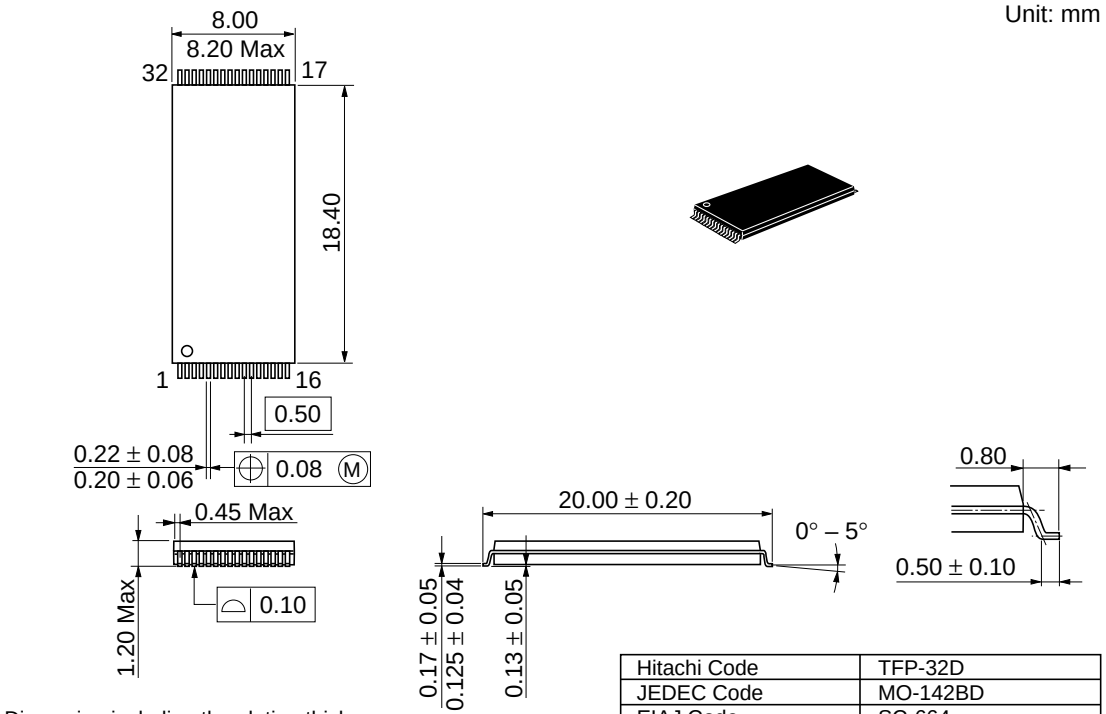


Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-32DC
JEDEC	—
EIAJ	—
Weight (reference value)	0.23 g

HM628128DLT Series (TFP-32D)

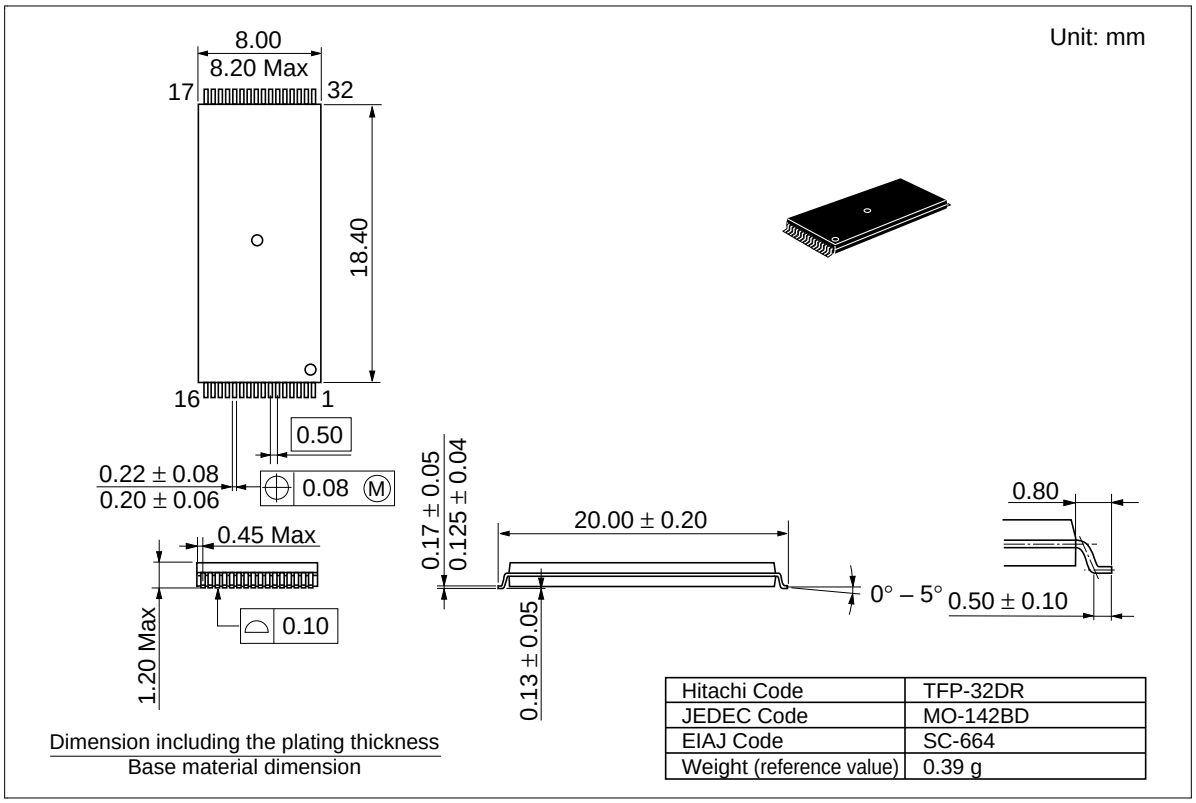
Unit: mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	TFP-32D
JEDEC Code	MO-142BD
EIAJ Code	SC-664
Weight (reference value)	0.39 g

HM628128DLR Series (TFP-32DR)



Hitachi Code	TFP-32DR
JEDEC Code	MO-142BD
EIAJ Code	SC-664
Weight (reference value)	0.39 g

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Revision Record

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0.0	Jan. 20, 1999	Initial issue		