NEC
ELECTRON DEVICE

DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC659

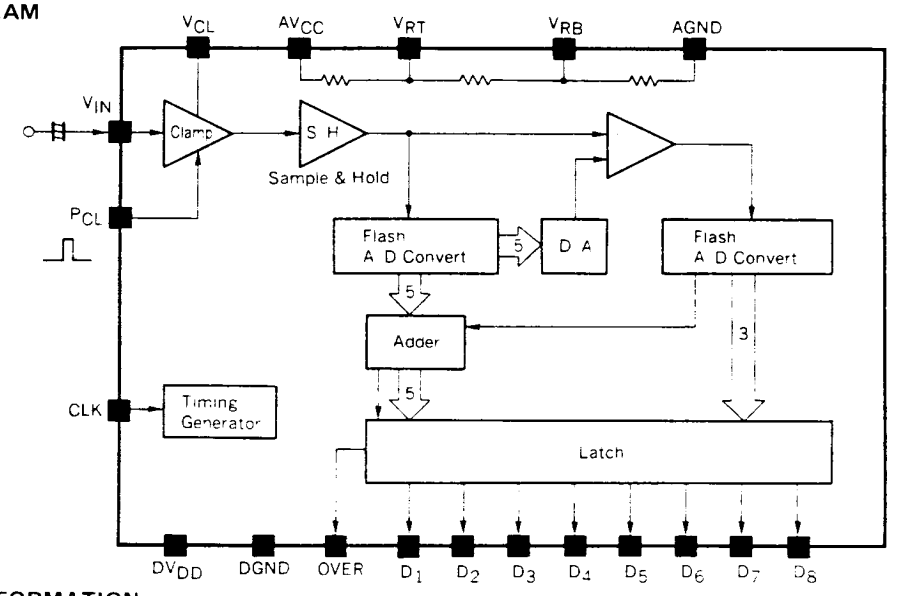
8 BIT A/D CONVERTER FOR VIDEO PROCESSING WITH REFERENCE GENERATOR AND CLAMP CIRCUIT

The μPC659 is a 8 bit A/D converter for video signal processing. The high speed and high quality Bipolar processing technology have enabled fast conversion rate and high resolution to be achieved. Conversion Rate is up to 20 MHz and Linearity Error within ±0.5 LSB while operating at low power consumption. Also, this IC include sample and hold circuit, clamp circuit and reference voltage generator, which enables simple external circuits to be constructed.

FEATURES

- Resolution: 8 bits
- Conversion Rate: 20 M_{sps} MAX.
- Differential Non-Linearity: ±0.5 LSB MAX.
- Power Supply Voltage: +5 V single
- Analog Input Voltage: 1.0 V_{p-p} TYP.
- Include Clamp Circuit (Clamp voltage and clamp pulse must be supplied.)
- Include Sample and Hold Circuit
- Include Reference Voltage Generator: V_{RT} = 3.3 V, V_{RB} = 2.3 V
- Low Power Consumption: 395 mW TYP.

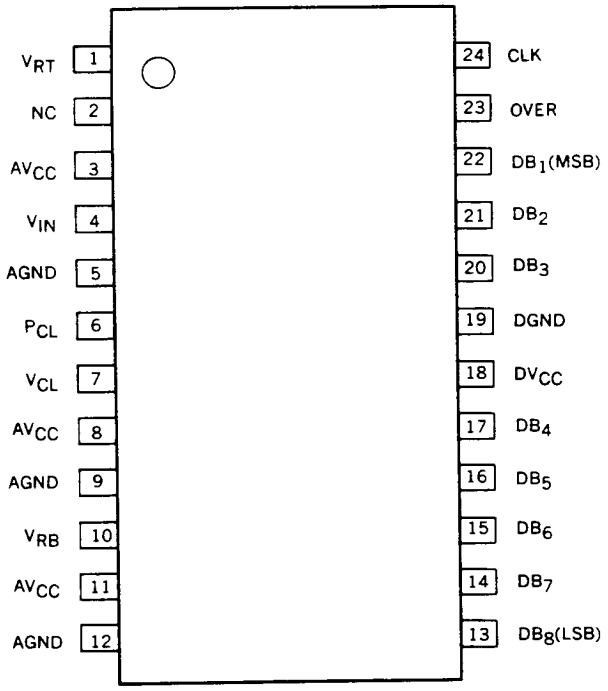
BLOCK DIAGRAM



ORDERING INFORMATION

ORDER NAME	PACKAGE
μPC659G	24 Pin Plastic SOP (300 mil)

CONNECTION DIAGRAM (Top View)



No.	Symbol	Pin Name	No.	Symbol	Pin Name
1	V_{RT}	Ref. Voltage (Top)	13	DB_8	Digital Data Output (LSB)
2	NC	No Connection	14	DB_7	Digital Data Output (7th)
3	AV_{CC}	Power Supply for Analog Circuit	15	DB_6	Digital Data Output (6th)
4	V_{IN}	Analog Signal Input Terminal	16	DB_5	Digital Data Output (5th)
5	AGND	Ground for Analog Circuit	17	DB_4	Digital Data Output (4th)
6	P_{CL}	Clamp Pulse Input Terminal	18	DV_{CC}	Power Supply for Digital Circuit
7	V_{CL}	Clamp Voltage Input Terminal	19	DGND	Ground for Digital Circuit
8	AV_{CC}	Power Supply for Analog Circuit	20	DB_3	Digital Data Output (3rd)
9	AGND	Ground for Analog Circuit	21	DB_2	Digital Data Output (2nd)
10	V_{RB}	Ref. Voltage (Bottom)	22	DB_1	Digital Data Output (MSB)
11	AV_{CC}	Power Supply for Analog Circuit	23	OVER	Digital Over Range Output
12	AGND	Ground for Analog Circuit	24	CLK	Sampling Clock Input Terminal

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	A, DV_{CC}	−0.3 to +6.0	V
Digital Input Voltage	V_{IND}	−0.3 to DV_{CC}+0.3	V
Analog Input Voltage	V_{INA}	−0.3 to AV_{CC}+0.3	V
Reference Input Voltage	V_{RT}, V_{RB}	−0.3 to AV_{CC}+0.3	V
Clamp Voltage	V_{CL}	−0.3 to AV_{CC}+0.3	V
Clamp Pulse Input Voltage	V_{PCL}	−0.3 to AV_{CC}+0.3	V
Operating Temperature	T_{opt}	−20 to +70	°C
Storage Temperature	T_{stg}	−40 to +150	°C

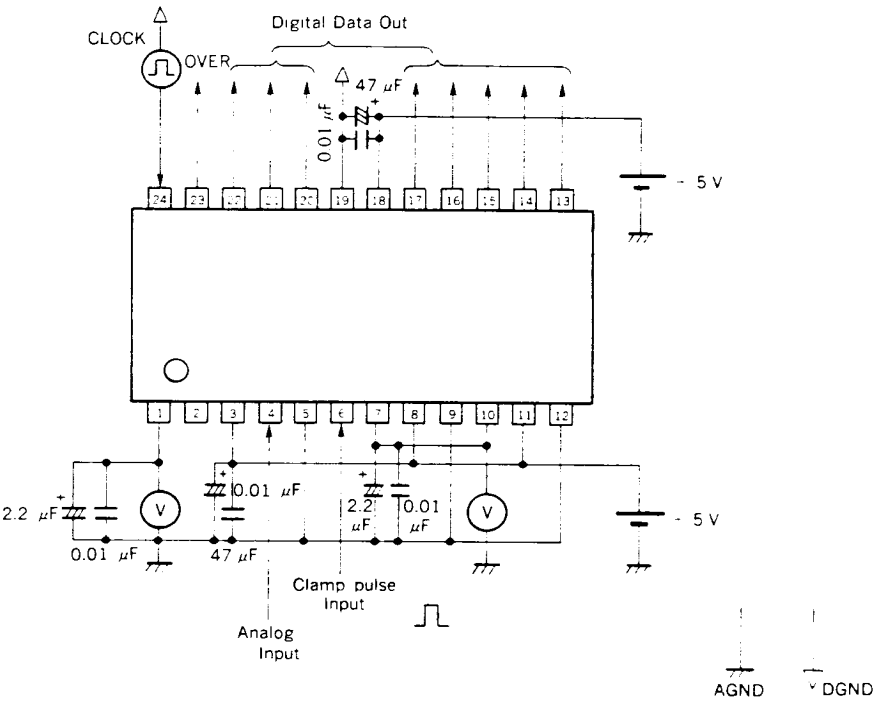
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to + 70 °C)

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	AV_{CC}, DV_{CC}	4.7	5.0	5.3	V	AGND = DGND = 0
Analog Input Voltage	V_{INA}	V_{RB}−0.4		V_{RT}+0.4	V	V_{CC} = 5.0 V
Clamp Input Voltage	V_{CL}	V_{RB}−0.4		V_{RT}+0.4	V	V_{CC} = 5.0 V
Sampling Clock	f_{SAMP}	1.0		20	MHz	
Sampling Clock Low Pulse Width	t_{PWL}	25			ns	
Sampling Clock High Pulse Width	t_{PWH}	25			ns	
Clock Input High Level Voltage	V_{CKH}	2.0			V	
Clock Input Low Level Voltage	V_{CKL}			0.8	V	
Clamp Pulse Width	t_{PWCL}	1.0			μs	
Clamp Pulse High Level Voltage	V_{PCLH}	2.0			V	
Clamp Pulse Low Level Voltage	V_{PCLL}			0.8	V	
Clamp Capacitance	C_{CL}		10		μF	
Maximum Analog Input Frequency	f_{AIN}		8.0	5.0	MHz	−3 dB Point

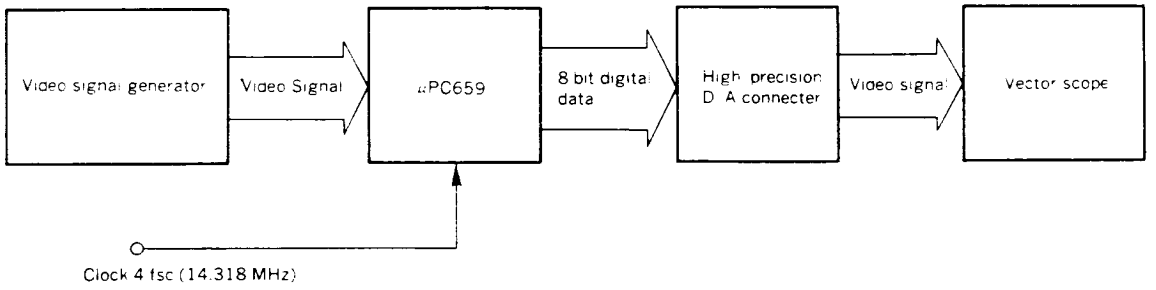
ELECTRICAL CHARACTERISTICS (T_a = −20 to + 70 °C AV_{CC} = DV_{CC} = 5.0±0.3 V)

TITLE	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Current	I_{CC}	50	79	110	mA	V_{CC} = 5.0 V, T_a = 25 °C
Resolution	RES		8		bit	
Non-linearity	NL			±1.5	LSB	V_{CC} = 5.0 V, T_a = 25 °C V_{IN} = 1.0 V_{P-P}
Differential Non-linearity	DNL			±0.5	LSB	V_{CC} = 5.0 V, T_a = 25 °C V_{IN} = 1.0 V_{P-P}
Differential Gain	DG		1.5	3.0	%	f_{SAMP} = 14.318 MHz NTSC Ramp wave (40 IRE)
Differential Phase	DP		0.8	3.0	deg	f_{SAMP} = 14.318 MHz NTSC Ramp wave (40 IRE)
Digital Data Output Delay Time	t_D		12	20	ns	Delay time from falling edge of sampling clock.
Digital Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA D_1 to D_8, OVER
Digital Output High Voltage	V_{OH}	2.7			V	I_{OH} = −400 μA D_1 to D_8, OVER
Digital Input Low Input Current	I_{INDL}			−200	μA	V_{IN} = 0.8 V
Digital Input High Input Current	I_{INDH}			10	μA	V_{IN} = 2.0 V
Analog Input Current	I_{INA}		10	35	μA	Measure input current from analog input terminal.
Reference Voltage (Bottom)	V_{RB}	2.1	2.3	2.5	V	V_{CC} = 5.0 V
Reference Voltage (Top)	V_{RT}	3.1	3.3	3.5	V	V_{CC} = 5.0 V
Analog Input Equivalent Capacitance	C_{IN}		3.0		pF	V_{IN} = V_{RB}
Clock Input Equivalent Capacitance	C_{CLK}		2.0		pF	
Reference Voltage (Difference)	V_{REF}		1.0		V	V_{RT}−V_{RB}, V_{CC} = 5.0 V

TEST CIRCUIT

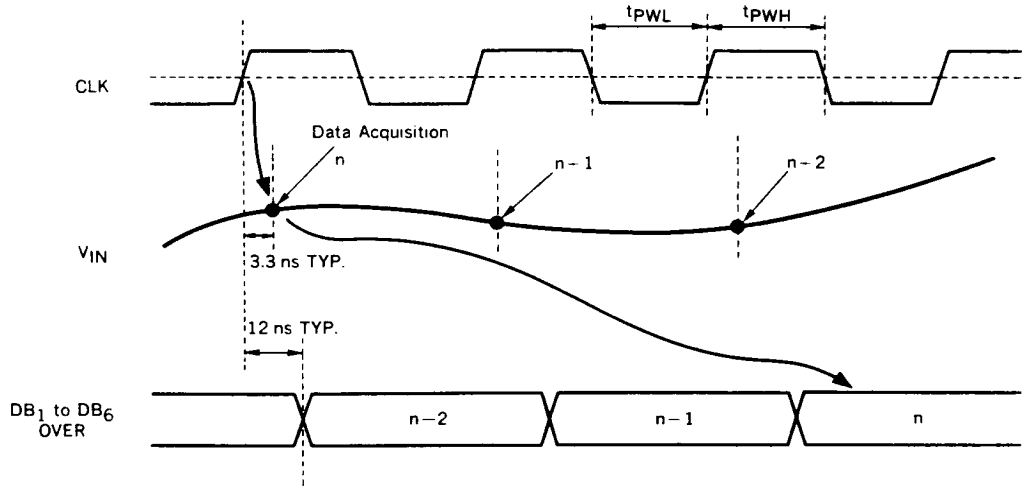


DG, DP TEST BLOCK



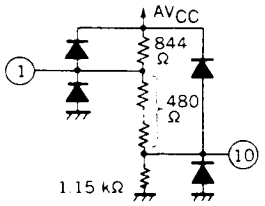
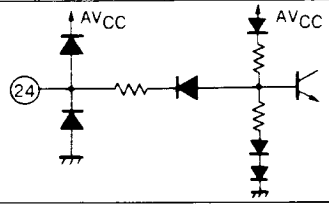
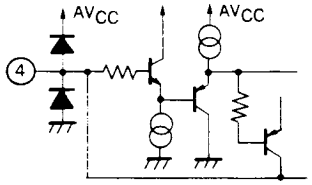
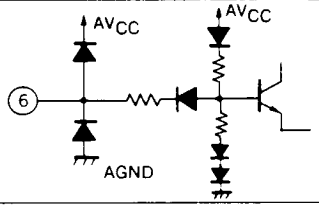
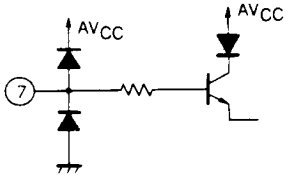
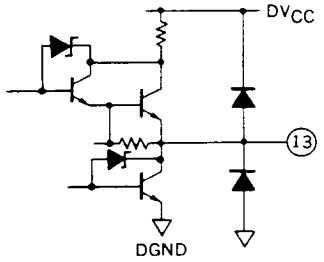
The video signal from the video signal generator is 40 IRE Ramp signal.

TIMING CHART



Analog signal is sampled with sampling clock and after the acquisition time (3.3 ns TYP.) started to be sampled. And converted data will be out after 2 sampling clock synchronized with the rise edge of sampling clock. Delay time from the rise edge of sampling clock is typically 12 ns.

EQUIVALENT CIRCUIT AROUND TERMINAL

Pin No.	Equivalent Circuit	Function
1, 10		1: Reference voltage (Top) V_{RT} 10: Reference voltage (Bottom) V_{RB}
5, 9, 12		Ground for Analog Circuit.
24		Sampling Clock input terminal. Analog data acquisition and digital data out are synchronized with the rise edge of this clock.
3, 8, 11		Power supply for analog circuit.
4		Analog signal input terminal. Input analog signal from this terminal. The clamp function also will be worked on this terminal. So it's necessary to connect capacitance and low impedance source.
6		Clamp pulse input terminal. Analog signal input from analog input terminal is clamped to the voltage; V_{CL} according to the high level term of this pulse.
7		Clamp bias input terminal. Analog input signal is clamped nearly to this input voltage; V_{CL} according to the clamp pulse; P_{CL} high level period.
13 to 17 21 to 22 23		Digital data output terminal. 13: Out of LSB data 14: Out of 7th data 15: Out of 6th data 16: Out of 5th data 17: Out of 4th data 20: Out of 3rd data 21: Out of 2nd data 22: Out of MSB data 23: Out of Over Flow (Active High)
18		Power supply for digital.
19		Ground for digital.

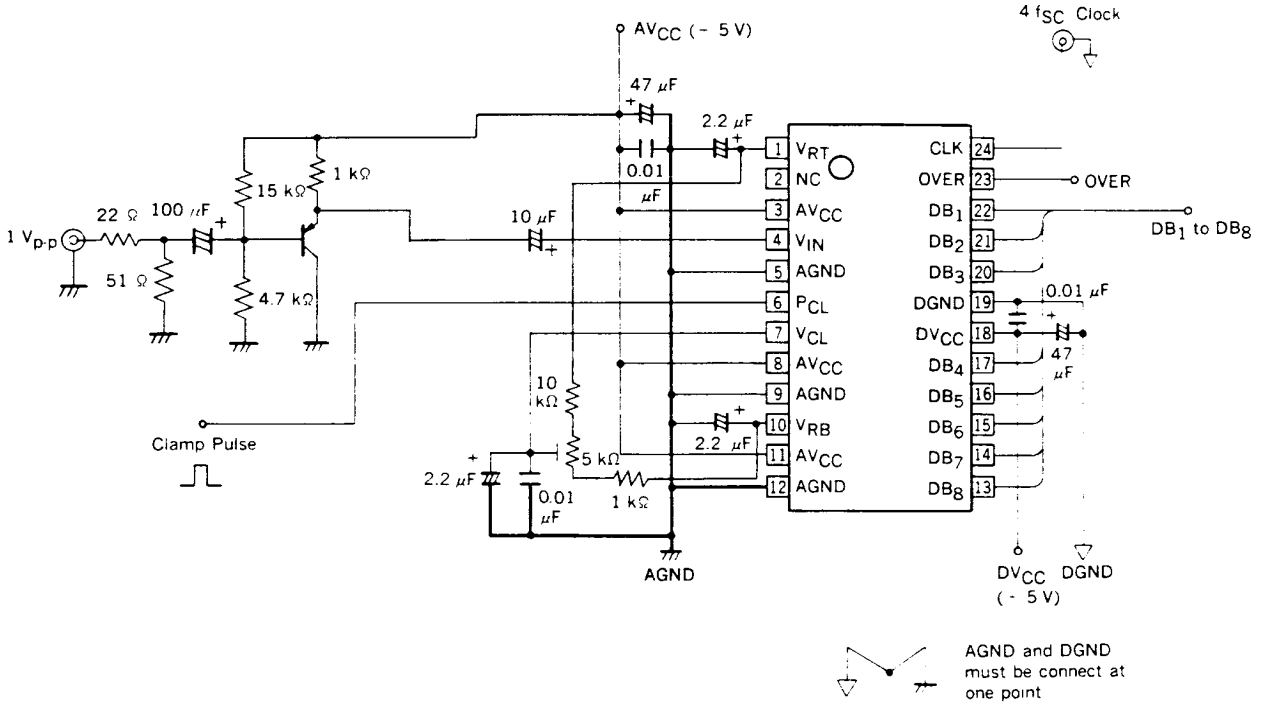
OUTPUT CODE FOR ANALOG INPUT

ANALOG INPUT	OUTPUT DIGITAL CODE								
	OVER	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)
V_{RB} to ½ LSB	0	0	0	0	0	0	0	0	0
½ LSB to (1+½) LSB	0	0	0	0	0	0	0	0	1
to	to	to	to	to	to	to	to	to	to
(254+½) LSB to (255+½) LSB	0	1	1	1	1	1	1	1	1
(255+½) LSB to V_{RT}	1	1	1	1	1	1	1	1	1
V_{RT} to AV_{CC}	1	1	1	1	1	1	1	1	1

$$LSB \fallingdotseq \frac{V_{RT}-V_{RB}}{256} \fallingdotseq 3.906 \text{ mV TYP.}$$

V_{RB} = 2.3 V TYP.
V_{RT} = 3.3 V TYP.

APPLICATION

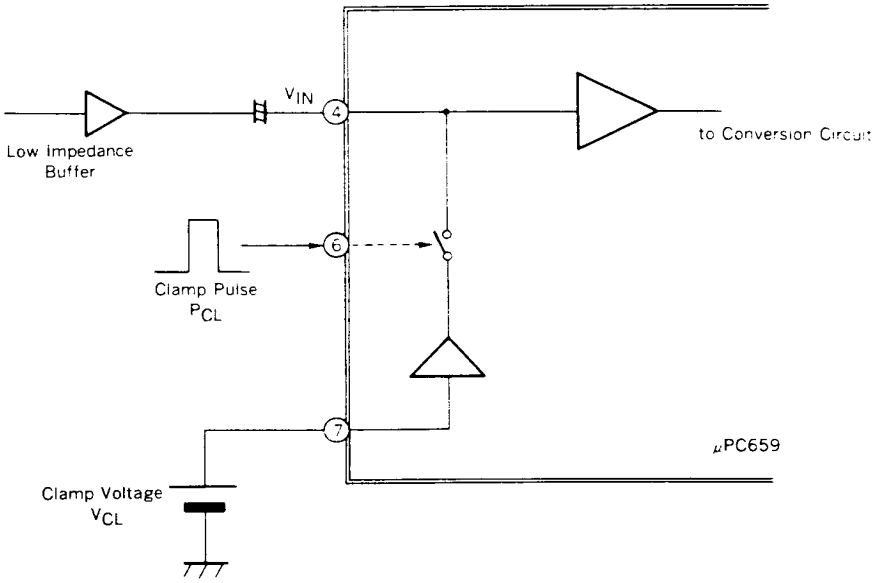


The application circuits and circuit constant described in this document don't apply to mass production where variations in parts quality and/or temperature characteristics are considered.

ATTENTION FOR APPLICATION

- Analog input terminal

  Please connect low impedance signal source to analog input terminal.
  And must be AC coupled. Clamp circuit is appeared by following rough block diagram.



- If don't use the clamp circuit

  The clamp pulse terminal (PIN 6) and GND must be short-circuit. And insert by-pass capacitor of about 0.1 μF between the clamp voltage input terminal (PIN 7) and GND.

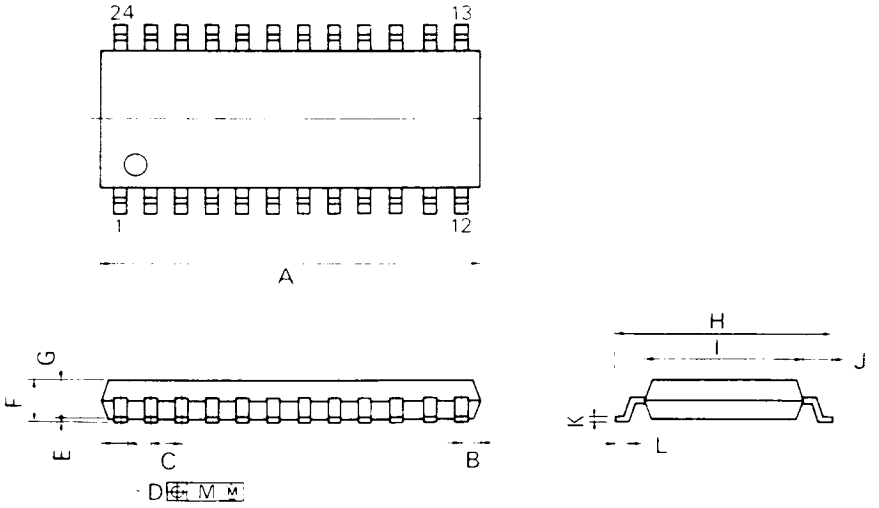
- Clamp voltage

  There is a few difference clamp voltage between the supply clamp voltage V_{CL} (PIN 7) and really clamp voltage.
  Really clamp voltage = $V_{CL} + \alpha$
  Take account of the α (about ±20 mV) at supply V_{CL} to PIN 7

- Power supply lines for analog circuit and digital circuit

  Must be thick line wiring for the power supply lines. And reduce the resistance and reactance ingredient the power supply lines.
  AV_{CC} and DV_{CC} must be connect at one point.
  AGND and DGND must be connect at one point.

24 PIN PLASTIC SOP (300 mil)



P24GM-50-300B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7 ± 0.3	$0.303^{+0.012}_{-0.012}$
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005