

# TC9198P, TC9198F

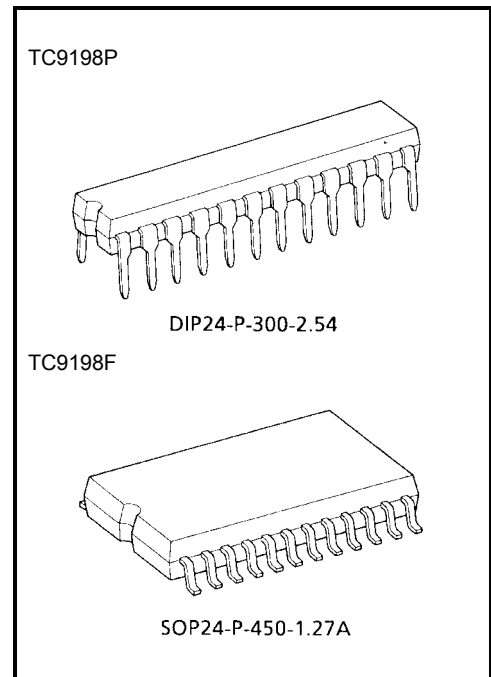
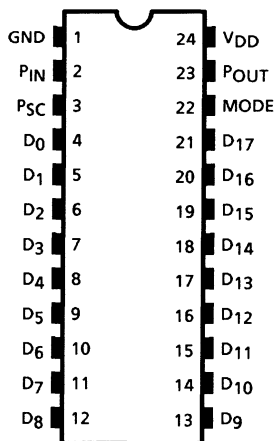
## Programmable Counter

TC9198P, TC9198F are high speed programmable counters developed for dividing PLL circuits and other various circuits.

### Features

- Setting of number of divisions can be made directly from the input terminals.
- The counter allows changing-over of swallow system/simple division.
- At simple division, changing-over of BCD code/BINARY code can be performed.
- The number of division is 262, 143 in maximum in swallow mode, and can be 5 to 65,535 at BINARY in simple division mode and can be 5 to 15,999 at BCD code.
- Owing to CMOS construction, the operating power voltage range is wide, and the power consumption is low.
- The package is DIP-24 pin for TC9198P and SOP-24 pin for TC9198F.

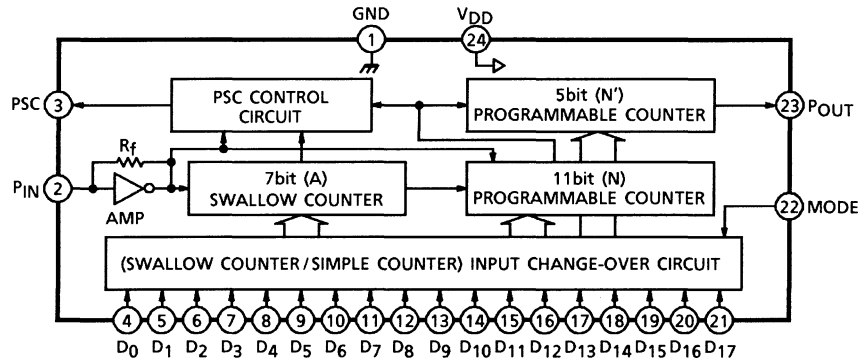
### Pin Assignment (top view)



#### Weight

DIP24-P-300-2.54: 1.2 g (typ.)  
SOP24-P-450-1.27A: 0.48 g (typ.)

Block Diagram



Pin Function

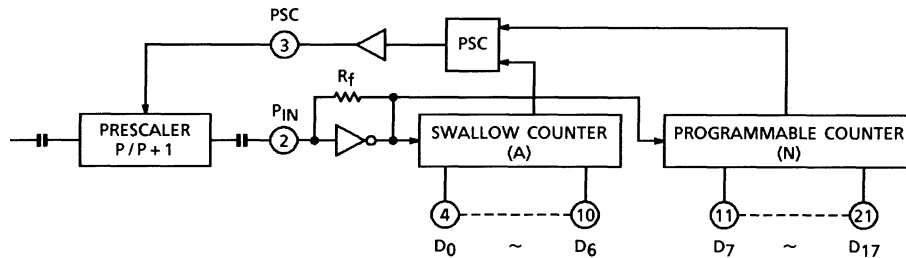
Pin No.	Symbol	Pin Name	Function and Operation	Note
1	GND	Ground Terminal	—	—
24	V <sub>DD</sub>	Power Supply Terminal		
2	P <sub>IN</sub>	Programmable Counter Input	Programmable counter input terminal. Prescaler output is input by the capacitor coupling.	Amp. Circuit built in
3	PSC	Prescaler Control Output	No. of division control signal output prescaler. It becomes P in "H" level, and P + 1 in "L" level.	—
22	MODE	Counter Operation Change-over Input	Change-over input for swallow counter operation and simple counter operation. It becomes swallow counter at "L" level, or open and simple counter operation at "H" level.	Pull down resistance built in
4	D <sub>0</sub>	Number of Division Setting Input	Input terminal for setting number of division of programmable counter. (1) MODE (22 pin) = at "L" level <ul style="list-style-type: none"> <li>D<sub>0</sub>~D<sub>6</sub> → Swallow counter: A</li> <li>D<sub>7</sub>~D<sub>17</sub> → Programmable counter: N</li> </ul> (2) MODE = at "H" and D <sub>17</sub> = at "L" level <ul style="list-style-type: none"> <li>Simple counter operation in setting BINARY code.</li> <li>D<sub>0</sub>~D<sub>15</sub> → Programmable counter: N</li> <li>D<sub>16</sub> → NC</li> </ul> (3) MODE = at "H" and D <sub>17</sub> = at "H" level <ul style="list-style-type: none"> <li>Simple counter operation in setting BCD code.</li> <li>D<sub>0</sub>~D<sub>3</sub> → N = 1~9 setting</li> <li>D<sub>4</sub>~D<sub>7</sub> → N = 10~90 setting</li> <li>D<sub>8</sub>~D<sub>11</sub> → N = 100~900 setting</li> <li>D<sub>12</sub>~D<sub>15</sub> → N = 1000~15000 setting</li> <li>D<sub>16</sub> → NC</li> </ul>	
5	D <sub>1</sub>			
6	D <sub>2</sub>			
7	D <sub>3</sub>			
8	D <sub>4</sub>			
9	D <sub>5</sub>			
10	D <sub>6</sub>			
11	D <sub>7</sub>			
12	D <sub>8</sub>			
13	D <sub>9</sub>			
14	D <sub>10</sub>			
15	D <sub>11</sub>			
16	D <sub>12</sub>			
17	D <sub>13</sub>			
18	D <sub>14</sub>			
19	D <sub>15</sub>			
20	D <sub>16</sub>			
21	D <sub>17</sub>			
23	P <sub>OUT</sub>	Programmable Counter Output Terminal	1/N of P <sub>IN</sub> input frequency is output pulse width corresponds to 4 cycles of input frequency.	—

**Description On Function and Operation**

**1. Programmable Counter**

When the MODE INPUT (pin 22) is set to “L” level (or opened), the programmable counter becomes swallow system.

The system consists of a 7 bit swallow counter, 11 bit programmable counter and a prescaler logic which change-over the number of divisions of the 2-module prescaler connected to the outside.



- Total number of divisions can be determined by the following formula  

$$\text{Number of divisions} = (P + 1) \cdot A + P \cdot (N - A)$$

$$= N \cdot P + A \quad \text{Where, } N > A$$
- The prescaler used requires to be the number of divisions of  $P + 1$  when the PSC terminal is in “L” level and of  $P$  when it is in “H” level.
- The input for setting the number of divisions of the programmable counter consists of 18 bits, but it should be cared that it changes by the number of divisions  $P$  of the prescaler used. ( $P \leq 128$ )

(1) When prescaler is  $P = 128$

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>	D <sub>16</sub>	D <sub>17</sub>
2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	2 <sup>4</sup>	2 <sup>5</sup>	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>	2 <sup>15</sup>	2 <sup>16</sup>	2 <sup>17</sup>

Note 1: The binary code D of the number of division is  $16,384 \leq D \leq 262,143$ , as a rule.

(2) When prescaler is  $P = 64$

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>	D <sub>16</sub>	D <sub>17</sub>
2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	2 <sup>4</sup>	2 <sup>5</sup>	“0”	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>	2 <sup>15</sup>	2 <sup>16</sup>

Note 2: The binary code D of the number of divisions is  $4,096 \leq D \leq 131,071$ , as a rule.

Note 3: D<sub>6</sub> (pin 10) are used as GND or in open.

(3) When prescaler is  $P = 32$

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>	D <sub>16</sub>	D <sub>17</sub>
2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	2 <sup>4</sup>	“0”	“0”	2 <sup>5</sup>	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>	2 <sup>15</sup>

Note 4: The binary code D of the number of divisions is  $1,024 \leq D \leq 65,535$ , as a rule.

Note 5: D<sub>5</sub> (pin 9) and D<sub>6</sub> (pin 10) are used as GND or in open.

(4) When prescaler is P = 16

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>	D <sub>16</sub>	D <sub>17</sub>
2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	"0"			2 <sup>4</sup>	2 <sup>5</sup>	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>

Note 6: The binary code D of the number of divisions is  $256 \leq D \leq 32,767$ , as a rule.

Note 7: D<sub>4</sub>~D<sub>6</sub> (pin 8~pin 9) are used as GND or in open.

## 2. Simple Program Counter

When the MODE INPUT (pin 22) is set to "H" level, the simple counter system is established.

When D<sub>17</sub> (pin 21) is made to "H" level, the system operates in BCD mode, and to "L" level, in BINARY mode.

(1) Operation in BINARY mode: D<sub>17</sub> (pin 21) = D<sub>16</sub> (pin 20) = "L" level or in open

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
2 <sup>0</sup>	2 <sup>1</sup>	2 <sup>2</sup>	2 <sup>3</sup>	2 <sup>4</sup>	2 <sup>5</sup>	2 <sup>6</sup>	2 <sup>7</sup>	2 <sup>8</sup>	2 <sup>9</sup>	2 <sup>10</sup>	2 <sup>11</sup>	2 <sup>12</sup>	2 <sup>13</sup>	2 <sup>14</sup>	2 <sup>15</sup>

Note 8: The BINARY code D of number of divisions becomes  $5 \leq D \leq 65,535$

(2) Operation in BCD mode: D<sub>17</sub> (pin 21) = "H", D<sub>16</sub> (pin 20) = "L" level or open

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
1	2	4	8	1	2	4	8	1	2	4	8	1	2	4	8

Note 9: D<sub>0</sub>~D<sub>3</sub>, D<sub>4</sub>~D<sub>7</sub>, D<sub>8</sub>~D<sub>11</sub> set number of divisions by BCD code.

It should be cared that it does not operate when it is set N = 10 or more.

Note 10: In D<sub>12</sub>~D<sub>15</sub>, the number of division can be set by the BINARY code.

D<sub>12</sub>~D<sub>15</sub> = 0101 (A) → N = 10,000

D<sub>12</sub>~D<sub>15</sub> = 1101 (B) → N = 11,000

D<sub>12</sub>~D<sub>15</sub> = 0011 (C) → N = 12,000

D<sub>12</sub>~D<sub>15</sub> = 1011 (D) → N = 13,000

D<sub>12</sub>~D<sub>15</sub> = 0111 (E) → N = 14,000

D<sub>12</sub>~D<sub>15</sub> = 1111 (F) → N = 15,000

Note 11: The BCD code of the number of divisions becomes  $5 \leq D \leq 15,999$

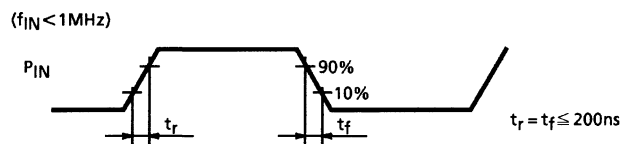
## Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>DD</sub>	-0.3~7.0	V
Input voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> + 0.3	V
Power dissipation	P <sub>D</sub>	300	mW
Operating temperature	T <sub>opr</sub>	-40~85	°C
Storage temperature	T <sub>stg</sub>	-65~150	°C

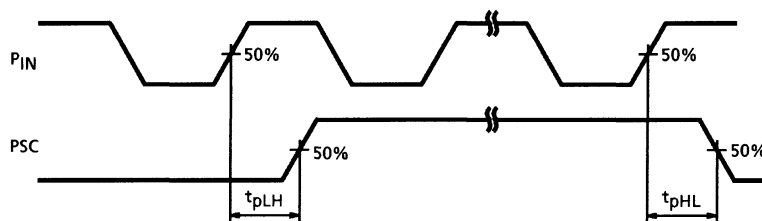
## Electrical Characteristics (unless otherwise specified, Ta = -40~85°C, V<sub>DD</sub> = 5.0 V)

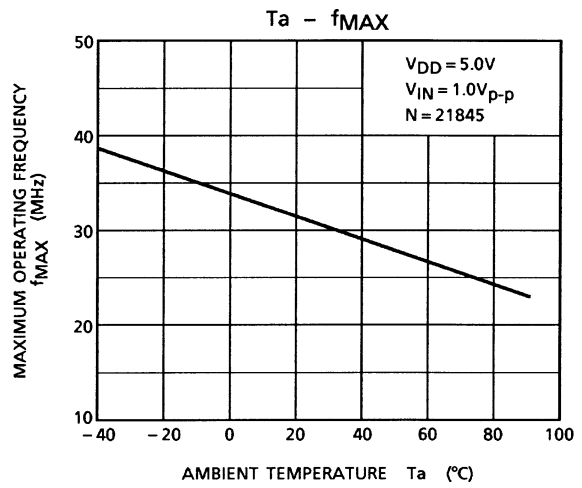
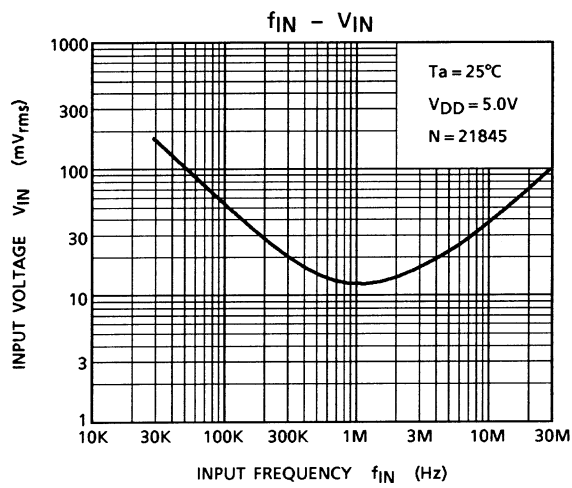
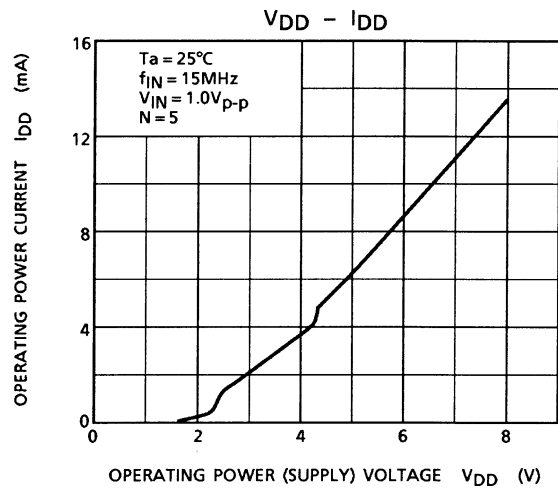
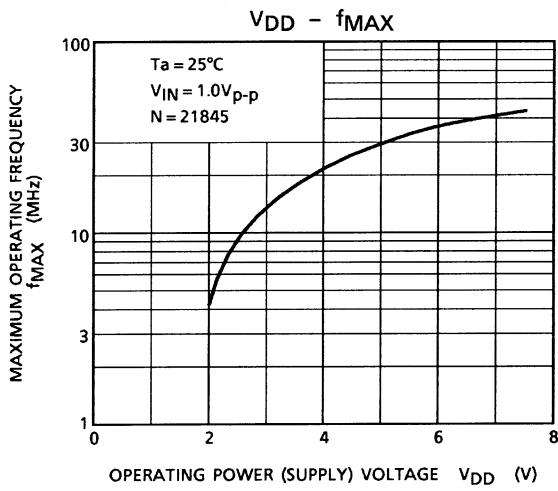
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage		V <sub>DD</sub>	—	f <sub>IN</sub> = 15 MHz, V <sub>IN</sub> = 1.0 V <sub>p-p</sub>	4.0	5.0	6.0	V
Operating supply current		I <sub>DD</sub>	—	f <sub>IN</sub> = 15 MHz, V <sub>IN</sub> = 1.0 V <sub>p-p</sub>	—	5.0	10	mA
Maximum operating frequency		f <sub>opr</sub> (1)	—	V <sub>IN</sub> = 1.0 V <sub>p-p</sub> , BINARY mode	1.0	—	15	MHz
		f <sub>opr</sub> (2)	—	V <sub>IN</sub> = 1.0 V <sub>p-p</sub> , BCD mode	1.0	—	15	
Minimum operating frequency		f <sub>MIN</sub>	—	V <sub>IN</sub> = 1.0 V <sub>p-p</sub> (Note 12)	—	0.5	1.0	kHz
Operating input amplitude		V <sub>IN</sub>	—	f <sub>IN</sub> = 15 MHz	1.0	~	V <sub>DD</sub> - 0.1	V <sub>p-p</sub>
Input voltage	"H" level	V <sub>IH</sub>	—	D <sub>0</sub> ~D <sub>17</sub> terminal MODE terminal	V <sub>DD</sub> × 0.7	~	V <sub>DD</sub>	V
	"L" level	V <sub>IL</sub>	—		0	~	V <sub>DD</sub> × 0.3	
Pull-down resistance		R <sub>DW</sub>	—			32	47	
Output current	"H" level	I <sub>OH</sub>	—	PSC, P <sub>OUT</sub> terminal	V <sub>OH</sub> = 4.0 V	0.5	1.0	mA
	"L" level	I <sub>OL</sub>	—		V <sub>OL</sub> = 1.0 V	0.5	1.0	
Input resistance		R <sub>f</sub>	—	P <sub>IN</sub> terminal	82	125	250	kΩ
Transfer time	"H" level	t <sub>pLH</sub>	—	P <sub>IN</sub> → PSC transfer time C <sub>L</sub> = 15 pF (Note 13)	—	100	200	ns
	"L" level	t <sub>pHL</sub>	—		—	100	200	

Note 12: At the test of the minimum operating frequency, the input waveform is specified as follows.



Note 13: P<sub>IN</sub> → PSC transfer time

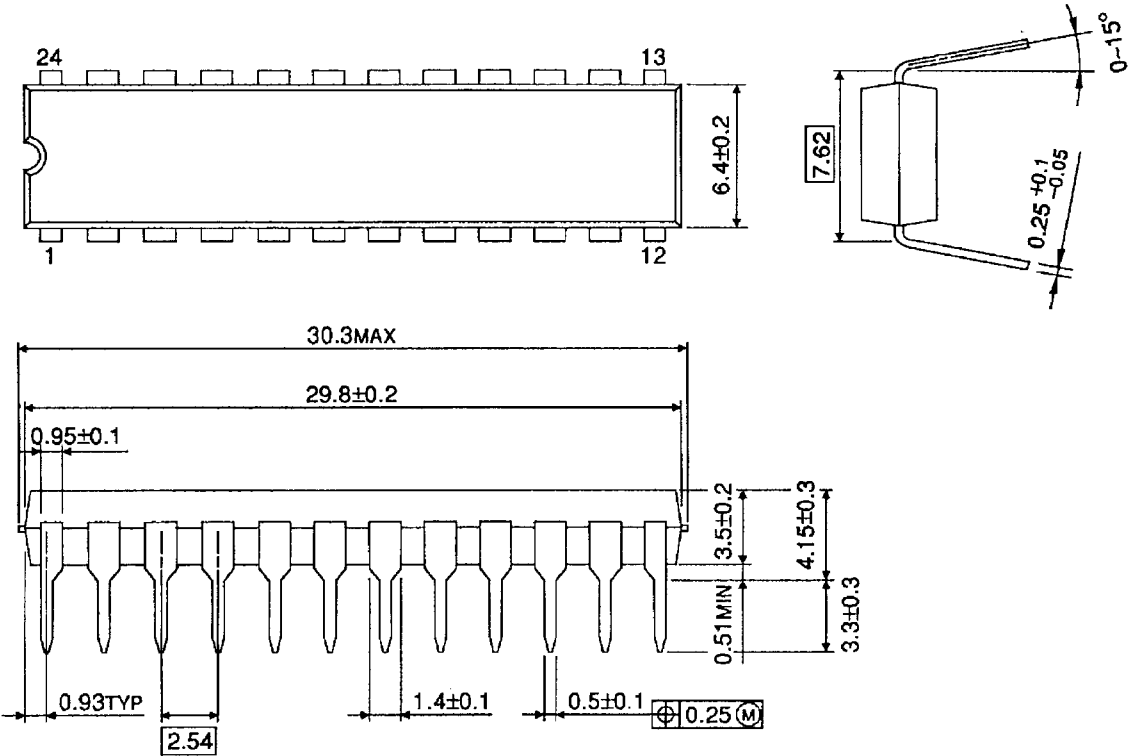




**Package Dimensions**

DIP24-P-300-2.54

Unit : mm

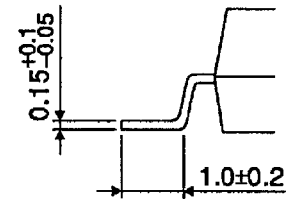
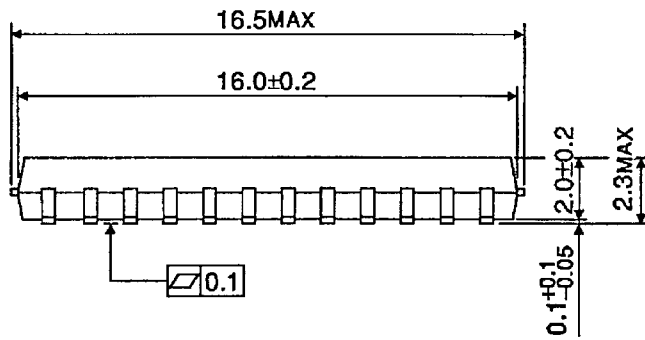
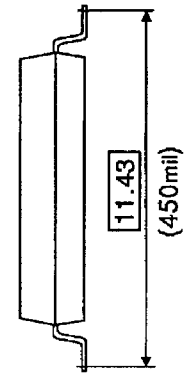
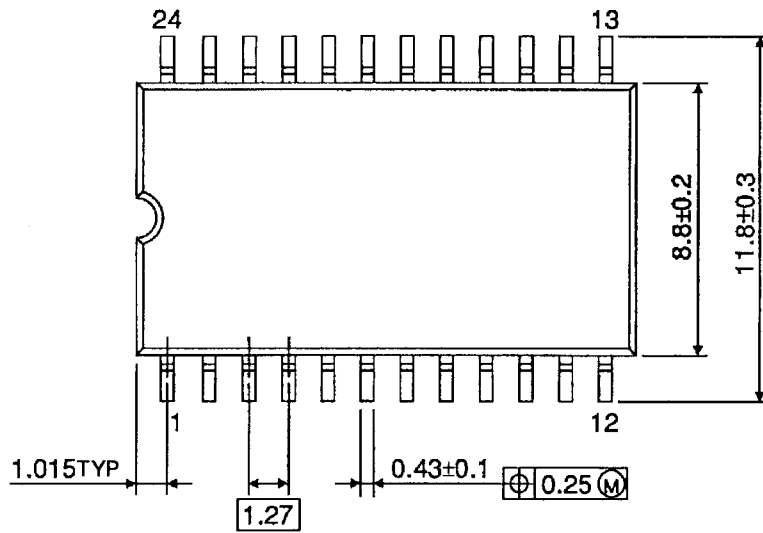


Weight: 1.2 g (typ.)

## Package Dimensions

SOP24-P-450-1.27A

Unit : mm



Weight: 0.48 g (typ.)



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