

## AD845

### FEATURES

Replaces Hybrid Amplifiers in Many Applications

#### AC PERFORMANCE:

Settles to 0.01% in 350 ns

100 V/ $\mu$ s Slew Rate

12.8 MHz Min Unity Gain Bandwidth

1.75 MHz Full Power Bandwidth at 20 V p-p

#### DC PERFORMANCE:

0.25 mV Max Input Offset Voltage

5  $\mu$ V/ $^{\circ}$ C Max Offset Voltage Drift

0.5 nA Input Bias Current

250 V/mV Min Open-Loop Gain

4  $\mu$ V p-p Max Voltage Noise, 0.1 Hz to 10 Hz

94 dB Min CMRR

Available in Plastic Mini-DIP, Hermetic CERDIP, and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard

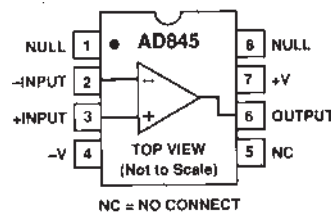
### GENERAL DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/ $\mu$ s, a stable unity gain bandwidth of 16 MHz, and a settling time of 350 ns to 0.01%—while driving a parallel load of 100 pF and 500  $\Omega$ —represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs that use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

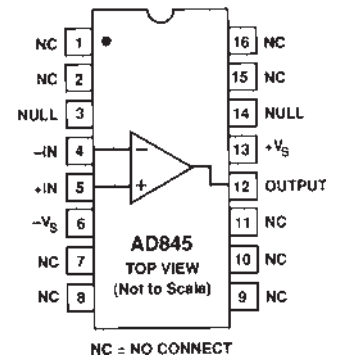
The AD845 is ideal for use in applications such as active filters, high speed integrators, photodiode preamps, sample-and-hold amplifiers, and log amplifiers, and for buffering A/D and D/A converters. The 250  $\mu$ V max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a  $\pm 10$  V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity gain buffer circuits.

### CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package  
and CERDIP (Q) Package



16-Lead SOIC  
(R-16) Package



The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 $^{\circ}$ C to 70 $^{\circ}$ C temperature range. AD845A and AD845B devices are specified for operation over the -40 $^{\circ}$ C to +85 $^{\circ}$ C industrial temperature range. The AD845S is specified to operate over the full military temperature range of -55 $^{\circ}$ C to +125 $^{\circ}$ C. Both the industrial and military versions are available in 8-lead CERDIP packages. The commercial version is available in an 8-lead plastic mini-DIP and 16-lead SOIC; J and S grade chips are also available.

### PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, HA2520, HA2522, HA2525, HA2620, HA2622, HA2625, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500  $\Omega$  loads.

# AD845—SPECIFICATIONS (@ 25°C and ±15 V dc, unless otherwise noted.)

Parameter	Conditions	AD845J/A			AD845K/B			AD845S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE <sup>1</sup>	$T_{MIN}$ to $T_{MAX}$	Initial Offset			0.1			0.25			mV
		0.7	1.5	2.5	0.1	0.25	0.4	0.25	1.0	2.0	mV
Offset Drift		20			1.5			5.0			$\mu\text{V}/^\circ\text{C}$
INPUT BIAS CURRENT <sup>2</sup>	$V_{CM} = 0\text{ V}$ $T_{MIN}$ to $T_{MAX}$	Initial			0.5			0.75			nA
		0.75	2	45/75	0.5	1	18/38	0.75	2	500	nA
INPUT OFFSET CURRENT	$V_{CM} = 0\text{ V}$ $T_{MIN}$ to $T_{MAX}$	Initial			15			25			pA
		25	300	3/6.5	15	100	1.2/2.6	25	300	20	nA
INPUT CHARACTERISTICS		Input Resistance			$10^{11}$			$10^{11}$			k $\Omega$
		Input Capacitance			4.0			4.0			pF
INPUT VOLTAGE RANGE	$V_{CM} = \pm 10\text{ V}$	Differential			$\pm 20$			$\pm 20$			V
		Common-Mode			$\pm 10$			$\pm 10$			V
		Common-Mode Rejection			+10.5/-13			+10.5/-13			dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	f = 10 Hz			4			4			$\mu\text{V p-p}$
		f = 100 Hz			80			80			$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz			60			60			$\text{nV}/\sqrt{\text{Hz}}$
		f = 10 kHz			25			25			$\text{nV}/\sqrt{\text{Hz}}$
		f = 100 kHz			18			18			$\text{nV}/\sqrt{\text{Hz}}$
		f = 100 kHz			12			12			$\text{nV}/\sqrt{\text{Hz}}$
		f = 1 kHz			0.1			0.1			$\text{pA}/\sqrt{\text{Hz}}$
OPEN-LOOP GAIN	$V_O = \pm 10\text{ V}$ $R_{LOAD} \geq 2\text{ k}\Omega$ $R_{LOAD} \geq 500\ \Omega$ $T_{MIN}$ - $T_{MAX}$	$R_{LOAD} \geq 2\text{ k}\Omega$			200			200			V/mV
		$R_{LOAD} \geq 500\ \Omega$			100			100			V/mV
		$T_{MIN}$ - $T_{MAX}$			70			70			V/mV
					500			500			
OUTPUT CHARACTERISTICS	$R_{LOAD} \geq 500\ \Omega$ Short Circuit Open Loop	Voltage			$\pm 12.5$			$\pm 12.5$			V
		Current			50			50			mA
		Output Resistance			5			5			$\Omega$
FREQUENCY RESPONSE	Unity Gain $V_O = \pm 10\text{ V}$ $R_{LOAD} = 500\ \Omega$	Small Signal			12.8			13.6			MHz
		Full Power Bandwidth <sup>3</sup>			16			16			MHz
		Rise Time			1.75			1.75			ns
		Overshoot			20			20			%
		Slew Rate			20			20			V/ $\mu\text{s}$
		Settling Time			80			94			
		10 V Step $C_{LOAD} = 100\text{ pF}$ $R_{LOAD} = 500\ \Omega$ to 0.01% to 0.1%			100			100			
			350			350			ns		
			250			250			ns		
DIFFERENTIAL GAIN	f = 4.4 MHz	0.04			0.04			0.04			%
DIFFERENTIAL PHASE	f = 4.4 MHz	0.02			0.02			0.02			Degree
POWER SUPPLY	$V_S = \pm 5$ to $\pm 15\text{ V}$ $T_{MIN}$ to $T_{MAX}$	Rated Performance			$\pm 15$			$\pm 15$			V
		Operating Range			$\pm 4.75$			$\pm 4.75$			V
		Rejection Ratio			$\pm 18$			$\pm 18$			dB
		Quiescent Current			88			88			mA
			110			110					
			10			10					
			12			12					

## NOTES

<sup>1</sup>Input offset voltage specifications are guaranteed after five minutes of operation at  $T_A = 25^\circ\text{C}$ .

<sup>2</sup>Bias current specifications are guaranteed maximum at either input after five minutes of operation at  $T_A = 25^\circ\text{C}$ .

<sup>3</sup>FPBW = slew rate/ $2\pi$  V peak.

<sup>4</sup>S grade  $T_{MIN}$ - $T_{MAX}$  are tested with automatic test equipment at  $T_A = -55^\circ\text{C}$  and  $T_A = +125^\circ\text{C}$ .

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage . . . . .	±18 V
Internal Power Dissipation <sup>2</sup>	
Plastic Mini-DIP . . . . .	1.6 W
CERDIP . . . . .	1.4 W
16-Lead SOIC . . . . .	1.5 W
Input Voltage . . . . .	+V <sub>S</sub>
Output Short-Circuit Duration . . . . .	Indefinite
Differential Input Voltage . . . . .	+V <sub>S</sub> and -V <sub>S</sub>
Storage Temperature Range	
Q . . . . .	-65°C to +150°C
N, R . . . . .	-65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . .	300°C

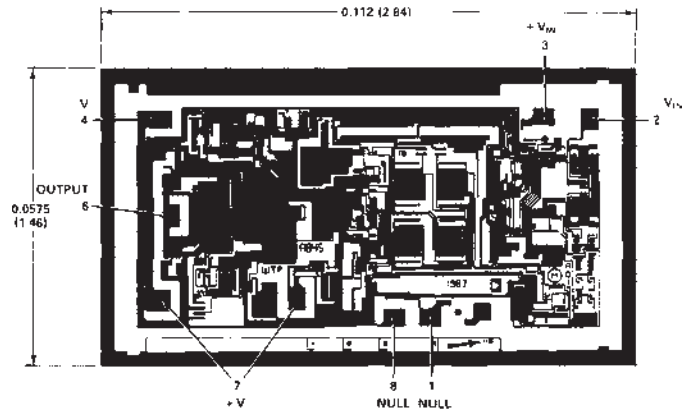
## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Mini-DIP package:  $\theta_{JA} = 100^\circ\text{C}/\text{W}$ ; CERDIP package:  $\theta_{JA} = 110^\circ\text{C}/\text{W}$ ; SOIC package:  $\theta_{JA} = 100^\circ\text{C}/\text{W}$ .

## METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).  
Contact factory for latest dimensions.



SUBSTRATE CONNECTED TO +V<sub>S</sub>

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option <sup>1</sup>
AD845JN	0°C to 70°C	8-Lead PDIP	N-8
AD845KN	0°C to 70°C	8-Lead PDIP	N-8
AD845JR-16	0°C to 70°C	16-Lead SOIC	R-16
AD845JR-16-REEL	0°C to 70°C	Tape and Reel	R-16
AD845JR-16-REEL7	0°C to 70°C	Tape and Reel	R-16
AD845AQ	-40°C to +85°C	8-Lead CERDIP	Q-8
AD845BQ	-40°C to +85°C	8-Lead CERDIP	Q-8
AD845SQ	-55°C to +125°C	8-Lead CERDIP	Q-8
AD845SQ/883B	-55°C to +125°C	8-Lead CERDIP	Q-8
5962-8964501PA <sup>2</sup>	-55°C to +125°C	8-Lead CERDIP	Q-8
AD845JCHIPS	0°C to 70°C	Die	

## NOTES

<sup>1</sup>N = Plastic DIP; Q = CERDIP; R = Small Outline IC (SOIC).

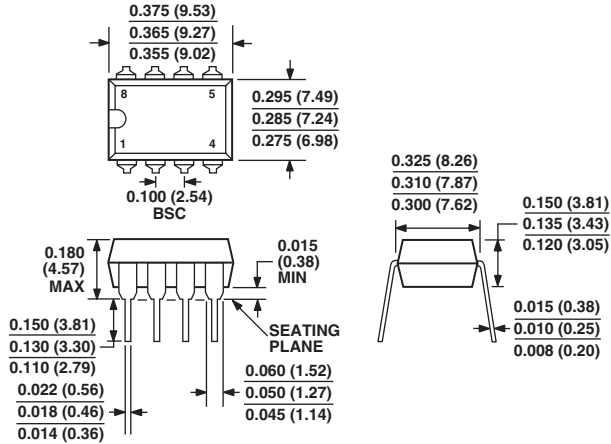
<sup>2</sup>See military data sheet.

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]

(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA

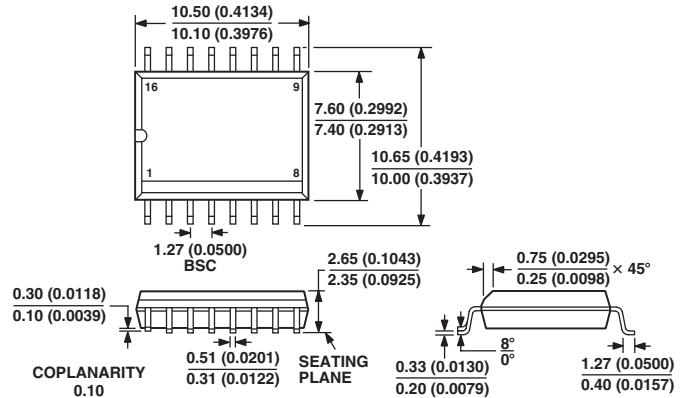
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16-Lead Standard Small Outline Package [SOIC]

Wide Body

(R-16)

Dimensions shown in millimeters and (inches)

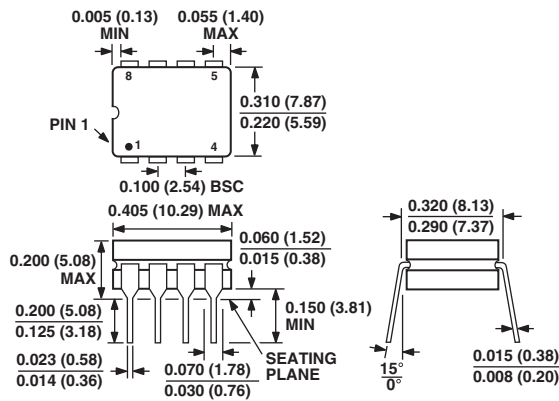


COMPLIANT TO JEDEC STANDARDS MS-013AA  
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8-Lead Ceramic Dual In-Line Package [CERDIP]

(Q-8)

Dimensions shown in inches and (millimeters)



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