Agilent Technologies

CMOS/TTL Compatible, Low Input Current, High Speed, High CMR Optocoupler

Technical Data

HCPL-7601
HCPL-7611

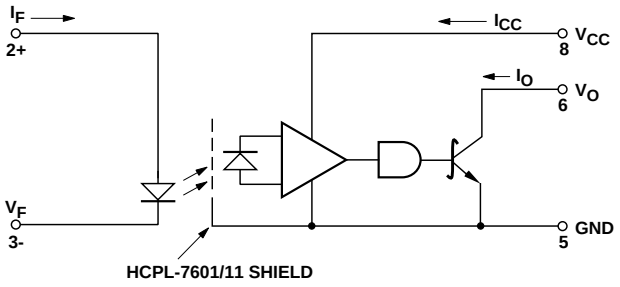
Features

- **Low Input Current Version of HCPL-2601/11 and 6N137**
- **Wide Input Current Range: I_F = 2 mA to 10 mA**
- **CMOS/TTL Compatible**
- **Guaranteed Switching Threshold: I_F = 2 mA (max.)**
- **Internal Shield for High Common Mode Rejection (CMR)**
  HCPL-7601: 5,000 V/µs (Typical) at V_{CM} = 50 V, I_F = 4 mA
  HCPL-7611: 15,000 V/µs (Typical) at V_{CM} = 1000 V, I_F = 4 mA
- **High Speed: 10 Mbd Typical**
- **Guaranteed ac and dc Performance Over Temperature: -40°C to 85°C**
- **VDE 0884 Approval: V_{IORM} = 600 V_{RMS}**
- **UL Recognized: 3750 V_{RMS}, 1 minute**
- **CSA Accepted**
- **Low Supply Current Requirement**
- **Low T_{PSK}: 40 ns Guaranteed**

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Programmable Logic Controllers**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Schematic



USE OF A 0.1 µF BYPASS CAPACITOR CONNECTED BETWEEN PINS 5 AND 8 IS REQUIRED (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

CAUTION: The small device geometries inherent to the design of this bipolar component increase the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Description

The HCPL-7601/11 is a low input current version of the HCPL-2601/11 and 6N137 (without enable). The optically coupled gates combine an AlGaAs high-efficiency light emitting diode and an integrated high gain photon detector to create a low input current device for low power applications. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 10,000 V/μs (HCPL-7611).

This unique design provides maximum ac and dc circuit isolation while achieving CMOS and TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to 85°C with no derating required allowing trouble free system performance. This product is suitable for high speed logic interfacing, input/output buffering, and applications that require low input-current switching levels.

The HCPL-7601/11 family offers many features that are especially beneficial to system designers. The low input current requirements and guaranteed switching threshold (2 mA max.) allows the LED to be driven directly by any standard high-speed CMOS gate (e.g. 74HC/HCT). This will simplify designs by eliminating the need for special driver circuits and result in lower part counts and greater system reliability while freeing up valuable printed circuit board space.

The wide current input range of 2 mA to 10 mA and guaranteed ac and dc performance over a wide temperature range will also simplify designs. Low supply current requirements mean lower power dissipation allowing for the use of a smaller, less expensive power supply. The high speed (10 Mbd typ.) and low propagation delay skew ($T_{psk} \leq 40$ ns guaranteed) allow for easier design of high speed parallel applications. The world-wide regulatory approval (UL/CSA/VDE 0884) will facilitate the acceptance of the end product in international markets.

Regulatory Information

The HCPL-7601 and HCPL-7611 have been approved by the following organizations:

UL–Approved under UL 1577, component recognition FILE E55361).

VDE–Approved according to VDE0884/08.87. This optocoupler is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Can be used for safe electrical separation between ac mains and SELV (safety extra-low voltage) in equipment according to the following specifications:
DIN VDE 0804/05.89
DIN VDE 0160/05.88

Reference voltage (VDE 011b Tab 4): 630 Vac.

CSA–Approved under CSA22.2 No. 0 - General Requirements, Canadian Electrical Code, Part II; and CSA Component Acceptance Notice #5, File CA 88324.

Absolute Maximum Ratings

(No Derating Required up to 85°C)
Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature .....260°C for 10 s
(1.6 mm below seating plane)
Average Input Current - I_F (See Note 2.) ..... 20 mA
Reverse Input Voltage - V_R ..... 3 V
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Collector Current - I_O ..... 50 mA
Output Collector Power Dissipation ..... 85 mW
Output Collector Voltage - V_O* ..... 7 V
Total Package Power Dissipation ..... 250 mW

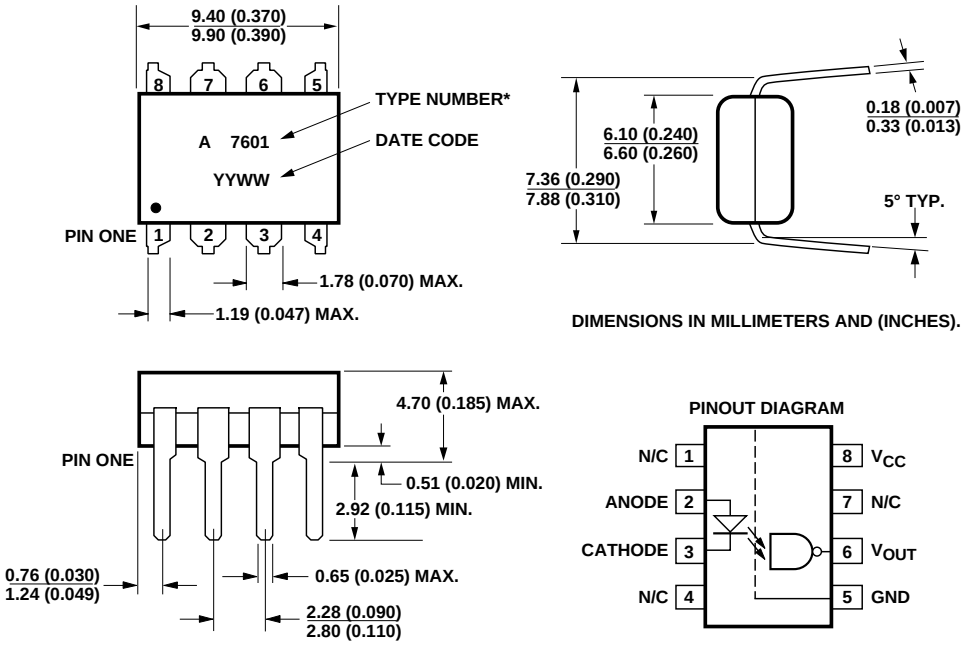
*Selection for higher output voltage up to 20 V is available.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Voltage, Low Level	V_{FL}	0	0.8	V
Input Current, High Level	I_{FH}	2	10	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out @ R_L= 1 kΩ	N		5	TTL Loads
Operating Temperature	T_A	-40	85	°C
Output Pull-up Resistor	R_L	330	4 k	Ω

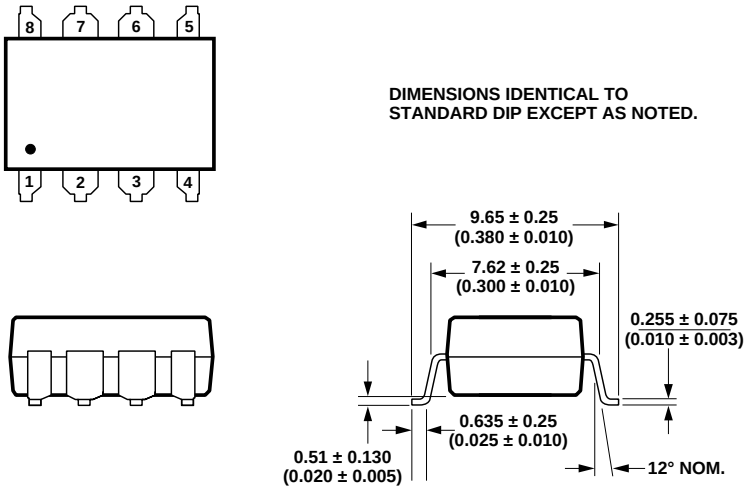
Package Outline Drawing

Standard DIP Package



*TYPE NUMBER FOR: HCPL-7601 = 7601
HCPL-7611 = 7611

Gull Wing Surface Mount Option 300*



* REFER TO OPTION 300 DATA SHEET
FOR MORE INFORMATION.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristics	Unit
Installation classification per DIN VDE 0109*/12.83, Table 1 for rated mains voltage ≤300V_{RMS} for rated mains voltage ≤600V_{RMS}		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0109/12.83)*		2	
Maximum Working Insulation Voltage	V_{IORM}	600	V_{RMS}
		848	V_{peak}
Input to Output Test Voltage, Method b** V_{PR} = 1.6 X V_{IORM} Production test with t_P = 1 sec, Partial discharge < 5 pC	V_{PR}	960	V_{RMS}
		1357	V_{peak}
Input to Output Test Voltage, Method a** V_{PR} = 1.2 X V_{IORM} Production test with t_P = 60 sec, Partial discharge < 5 pC	V_{PR}	720	V_{RMS}
		1018	V_{peak}
Highest Allowable Overvoltage** (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	6000	V_{peak}
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 16) Case Temperature Input Power Output Power	 T_{SI} $P_{SI,Input}$ $P_{SI,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V	R_{IS}	$\geq 10^{11}$	Ω

* This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V_{RMS} (per DIN VDE 0190/12.83).
**Refer to the front of the optocoupler section of the current Optoelectronics Designers Catalog for a more detailed description of VDE 0884 and other product safety regulations.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Clearance (External Air Gap)	L (IO1)	7.0	mm	Measured from input terminals to output terminals
Minimum External Creepage (External Tracking)	L (IO2)	8.0	mm	Measured from input terminals to output terminals
Minimum Internal Clearance (Internal Plastic Gap)		0.5	mm	Through insulation distance from conductor to conductor
Comparitive Tracking Index	CTI	175	V	DIN IEC 112/VDE 303 P1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group

Electrical Specifications

Over recommended temperature (T_A = -40°C to 85°C) unless otherwise specified. (See note 1.)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input Threshold Current	I_{TH}		1	2	mA	V_{CC} = 5.5V, $I_O \geq$ 13 mA, V_O = 0.6 V	5	
High Level Output Current	I_{OH}		3	100	µA	V_{CC} = 5.5 V, V_O = 5.5 V V_{FL} = 0.8 V	1	
Low Level Output Voltage	V_{OL}		0.35	0.6	V	V_{CC} = 5.5 V, I_F = 2 mA, I_{OL} (Sinking) = 13 mA	2, 4, 6	
High Level Supply Current	I_{CCH}		4.75	7	mA	V_{CC} = 5.5 V, I_F = 0 mA		
Low Level Supply Current	I_{CCL}		6	10	mA	V_{CC} = 5.5 V, I_F = 4 mA		
Input Forward Voltage	V_F	1.2	1.5	1.85	V	I_F = 4 mA	3	
Input Reverse Breakdown Voltage	BV_R	3			V	I_R = 100 µA		
Input Capacitance	C_{IN}		72		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		-1.6		mV/°C	I_F = 4 mA	3	
Input-Output Insulation	V_{ISO}	3750			V_{RMS}	RH ≤ 50%, t = 1 min. T_A = 25°C		3, 9
Resistance (Input-Output)	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 V		3
		10^{11}				T_A = 100°C, V_{I-O} = 500 V		
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 V_{dc}		3

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = -40°C to 85°C), V_{CC} = 5 V, C_L = 15 pF

Parameter	Symbol	Device	Min.	Typ.*	Max	Unit	Test Conditions		Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		25	58	75		T_A = 25°C	I_F = 2 mA, R_L = 1 kΩ	7, 8, 10	4, 10
					100					
			25	55	75	ns	T_A = 25°C	I_F = 4 mA R_L = 350 Ω		
					100					
Propagation Delay Time to Low Output Level	t_{PHL}		35	73	100		T_A = 25°C	I_F = 2 mA R_L = 1 kΩ	7, 9, 10	5, 10
					120					
			25	57	75		T_A = 25°C	I_F = 4 mA R_L = 350 Ω		
					100					
Pulse Width Distortion	$\|t_{PHL}-t_{PLH}\|$			16	55		I_F = 2 mA	R_L = 1 kΩ	11, 12	4, 5
				4	40		I_F = 4 mA	R_L = 350 Ω		
Propagation Delay Skew	t_{PSK}				75		I_F = 2 mA	R_L = 1 kΩ		6, 10
					40		I_F = 4 mA	R_L = 350 Ω		
Output Rise Time (10% - 90%)	t_{rise}			58			I_F = 2 mA	R_L = 1 kΩ	13	
				24			I_F = 4 mA	R_L = 350 Ω		
Output Fall Time (10% - 90%)	t_{fall}			10			I_F = 2 - 4 mA	R_L = 350 - 1 kΩ	13	
Common Mode Transient Immunity at High Output Level	CM_H	HCPL-7601	1,000	5,000		V/µs	V_{CM} = 50 V	I_F = 0 mA $V_{o(min)}$ = 2 V R_L = 350 - 1 kΩ T_A = 25°C	14	7
		HCPL-7611	10,000	15,000			V_{CM} = 1000 V			
Common Mode Transient Immunity at Low Output Level	CM_L	HCPL-7601	1,000	5,000			I_F = 2 - 4 mA R_L = 350 - 1 kΩ V_{CM} = 50 V	$V_{o(max)}$ = 0.8V T_A = 25°C	14	8
		HCPL-7611	2,000	5,000			I_F = 2 mA R_L = 1 kΩ V_{CM} = 1000 V			
			10,000	15,000			I_F = 4 mA R_L = 350 Ω V_{CM} = 1000 V			

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Notes:

1. Bypassing of the power supply line is required with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler, as illustrated in Figure 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 10 mm.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1 , 2, 3 and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
6. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the operating condition range.
7. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., $V_{OUT} > 2.0$ V).
8. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., $V_{OUT} < 0.8$ V). This specification assumes that good board layout procedures were followed to reduce the effective input/output capacitance as shown in Figure 15.
9. In accordance with UL and CSA requirements, each optocoupler is proof tested by applying an insulation test voltage ≥ 5000 Vrms for one second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
10. AC performance at $I_F = 4$ mA is approximately equivalent to the HCPL-2601/11 at $I_F = 7.5$ mA for comparison purposes.

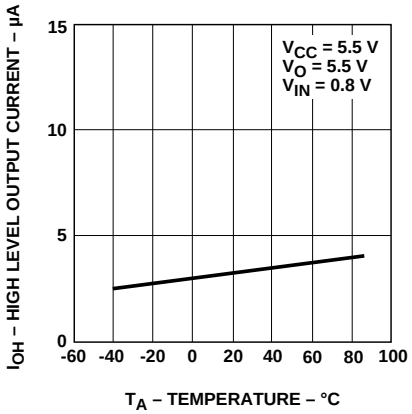


Figure 1. High Level Output Current vs. Temperature.

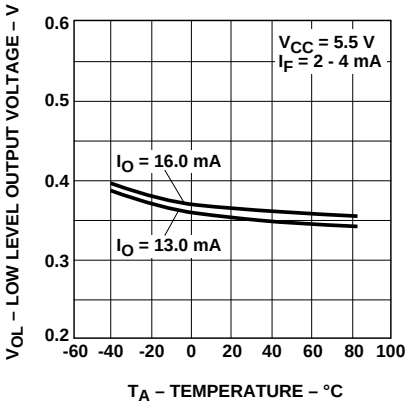


Figure 2. Low Level Output Voltage vs. Temperature.

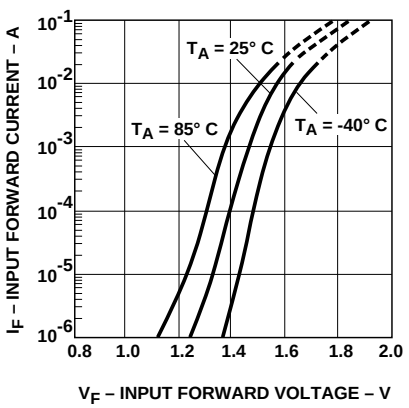


Figure 3. Typical Input Forward Current vs. Input Forward Voltage.

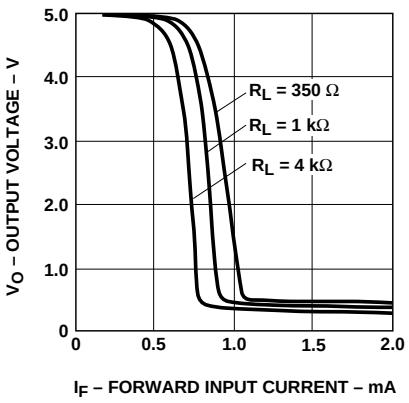


Figure 4. Output Voltage vs. Forward Input Current.

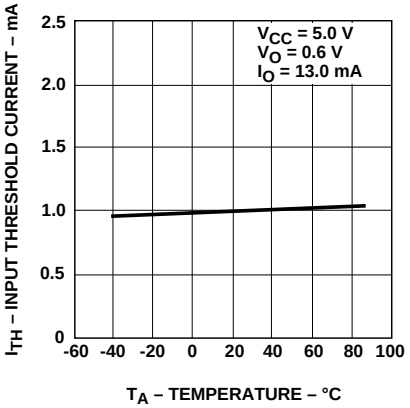


Figure 5. Input Threshold Current vs. Temperature.

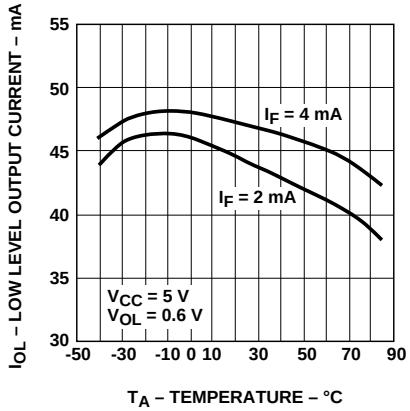


Figure 6. Low Level Output Current vs. Temperature.

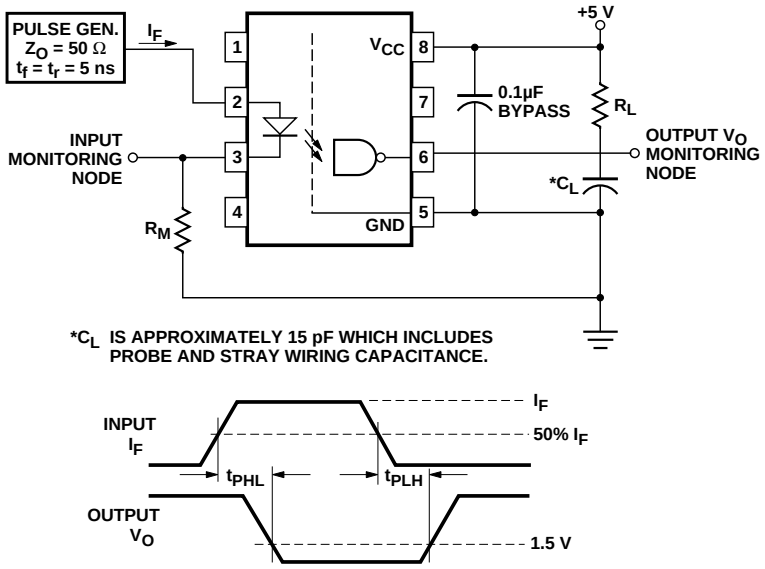


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.

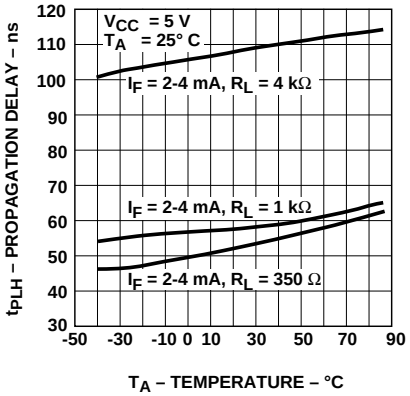


Figure 8. t_{PLH} – Propagation Delay vs. Temperature.

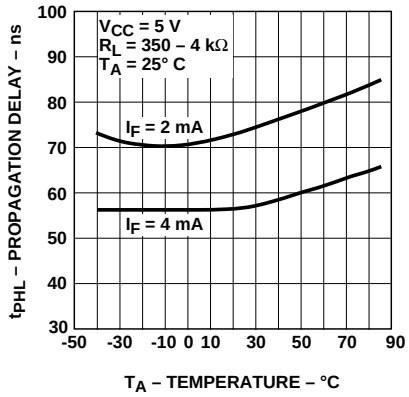


Figure 9. t_{PHL} – Propagation Delay vs. Temperature.

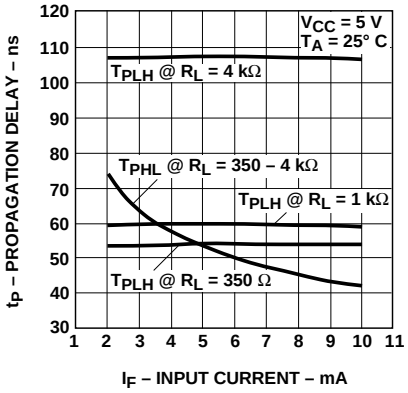


Figure 10. Propagation Delay vs. Input Current.

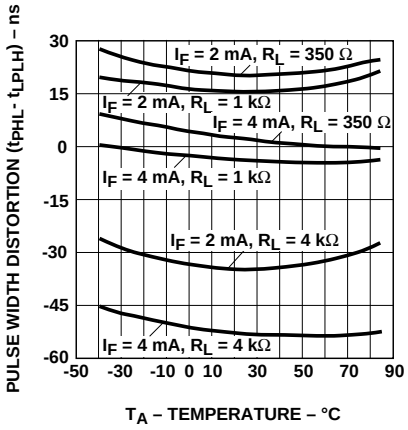


Figure 11. Pulse Width Distortion vs. Temperature.

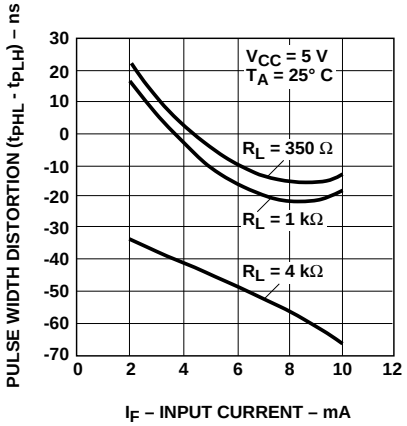


Figure 12. Pulse Width Distortion vs. Input Current.

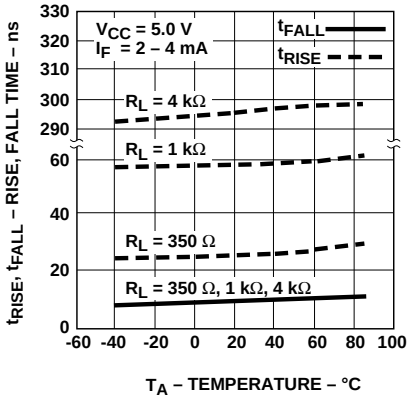


Figure 13. Rise and Fall Time vs. Temperature.

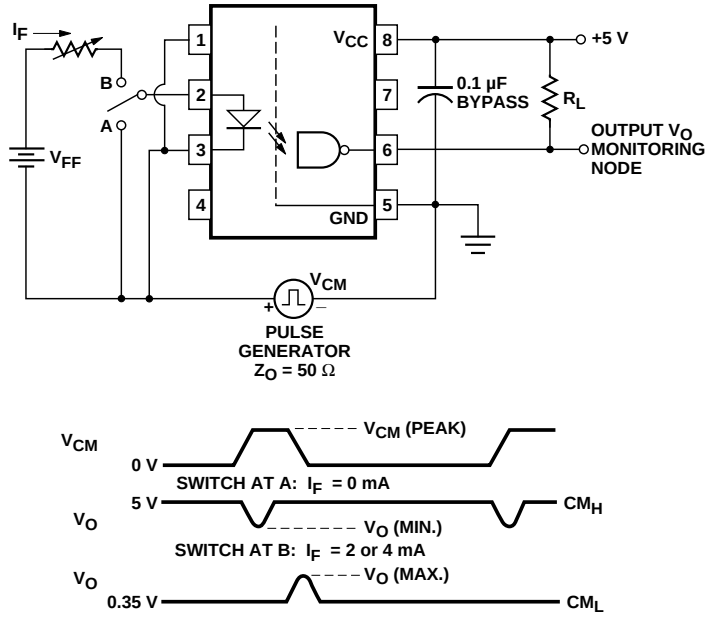


Figure 14. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

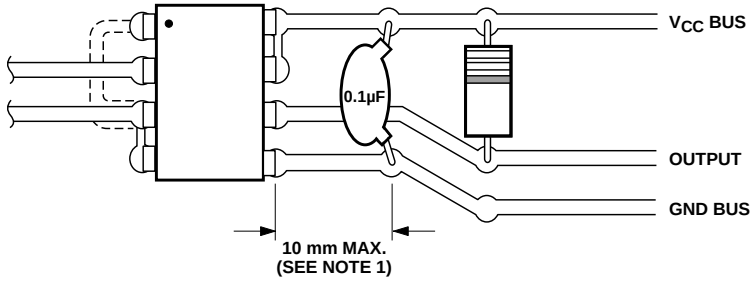


Figure 15. Recommended Printed Circuit Board Layout.

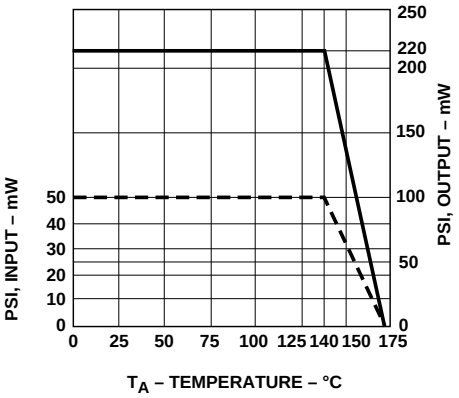


Figure 16. Dependence of Safety-Limiting Data on Ambient Temperature.

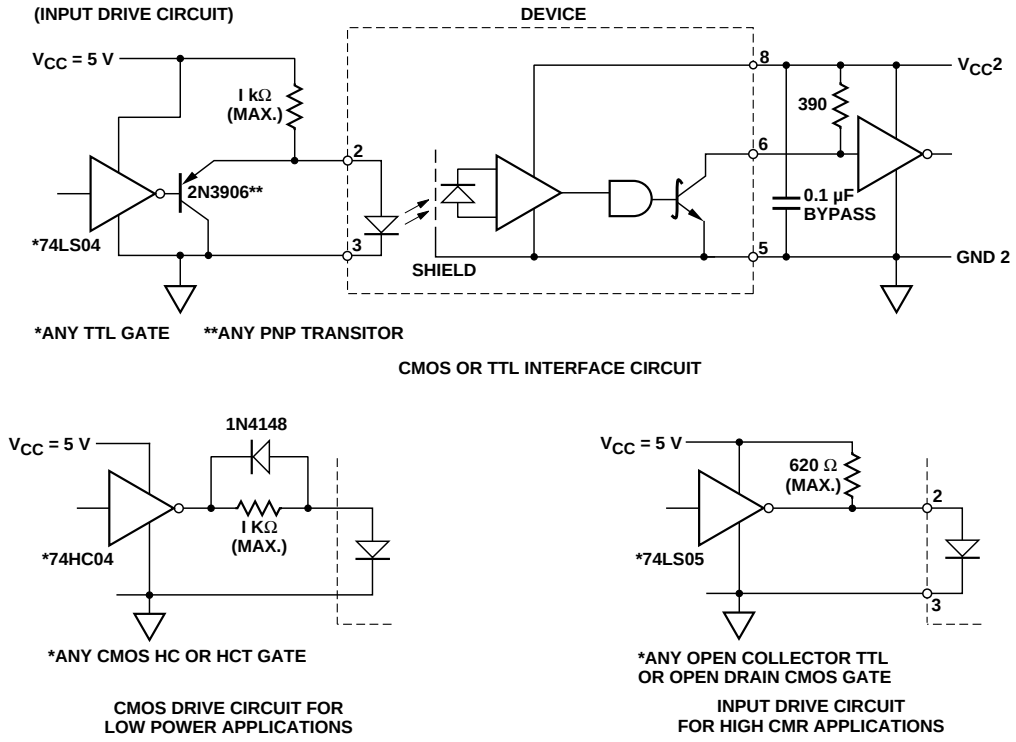


Figure 17. Recommended Interface Circuits.

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