

### 8-Bit Shift Register (S-In, P-Out)

The TC74HCT164A is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

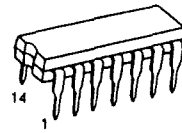
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding CLEAR input. Two serial data inputs (A, B) are provided so that one may be used as a data enable.

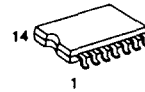
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

#### Features:

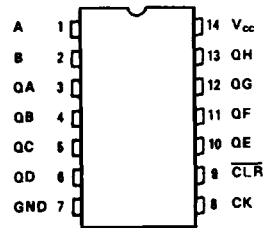
- High Speed:  $f_{MAX} = 61\text{MHz(Typ.)}$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation:  $I_{CC} = 4\mu\text{A(Max.)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IH} = 2\text{V(Min.)}$   
 $V_{IL} = 0.8\text{V(Max.)}$
- Wide Interfacing Ability: LSTTL, NMOS, CMOS
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance:  $I_{OH} = I_{OL} = 4\text{mA(Min.)}$
- Balanced Propagation Delays:  $t_{PLH} = t_{PHL}$
- Pin and Function Compatible with 74LS164



P

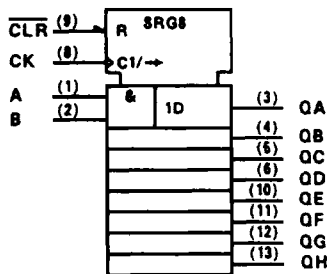


F



(TOP VIEW)

Pin Assignment



IEC Logic Symbol

Truth Table

Inputs				Outputs			
CLR	CK	Serial In		QA	QB	--	QH
		A	B				
L	X	X	X	L	L	-	L
H		X	X	No Change			
H		L	X	L	QAn	-	QGn
H		X	L	L	QAn	-	QGn
H		H	H	H	QAn	-	QGn

X: Don't Care

QAn - QGn: The level of QA - QG, respectively, before the most recent positive edge of the clock.

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	$V_{CC}$	-0.5 - 7	V
DC Input Voltage	$V_{IN}$	-0.5 - $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5 - $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	±20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	500(DIP)*/180(SOIC)	mW
Storage Temperature	$T_{stg}$	-65 - 150	°C
Lead Temperature 10sec	$T_L$	300	°C

\*500mW in the range of  $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

## Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	4.5 - 5.5	V
Input Voltage	$V_{IN}$	0 - $V_{CC}$	V
Output Voltage	$V_{OUT}$	0 - $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40 - 85	°C
Input Rise and Fall Time	$t_r, t_f$	0-500	ns

## DC Electrical Characteristics

Parameter	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		Unit		
			$V_{CC}$	Min.	Typ.	Max.	Min.		Max.	
High-Level Input Voltage	$V_{IH}$	-	4.5 ∫ 5.5	2.0	-	-	2.0	-	V	
Low-Level Input Voltage	$V_{IL}$	-	4.5 ∫ 5.5	-	-	0.8	-	0.8	V	
High-Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	4.5	4.5	4.5	-	4.4	-	V
			$I_{OH} = -4\text{mA}$	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	4.5	-	0.0	0.1	-	0.1	V
			$I_{OL} = 4\text{mA}$	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	-	-	±0.1	-	±0.1	μA	
			5.5	-	-	4.0	-	40.0		
Quiescent Supply Current	$\Delta I_{CC}$	Per Input: $V_{IN} = 0.5\text{V}$ or $2.4\text{V}$ Other Input: $V_{CC}$ or GND	5.5	-	-	2.0	-	2.9	mA	

Timing Requirements (Input  $t_r = t_f = 6\text{ns}$ )

Parameter	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~ 85°C		Unit
			V <sub>CC</sub>	Typ.	Limit	Limit	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	-	4.5	-	15	19	ns
			5.5	-	14	18	
Minimum Pulse Width (CLR)	$t_{W(H)}$	-	4.5	-	15	19	
			5.5	-	14	18	
Minimum Set-up Time (A, B)	$t_s$	-	4.5	-	10	13	
			5.5	-	9	11	
Minimum Hold Time (A, B)	$t_h$	-	4.5	-	0	0	
			5.5	-	0	0	
Minimum Removal Time (CLR)	$t_{rem}$	-	4.5	-	10	13	
			5.5	-	9	11	
Clock Frequency	f	-	4.5	-	30	24	MHz
			5.5	-	33	26	

AC Electrical Characteristics (C<sub>L</sub> = 15pF, V<sub>CC</sub> = 5V, Ta = 25°C)

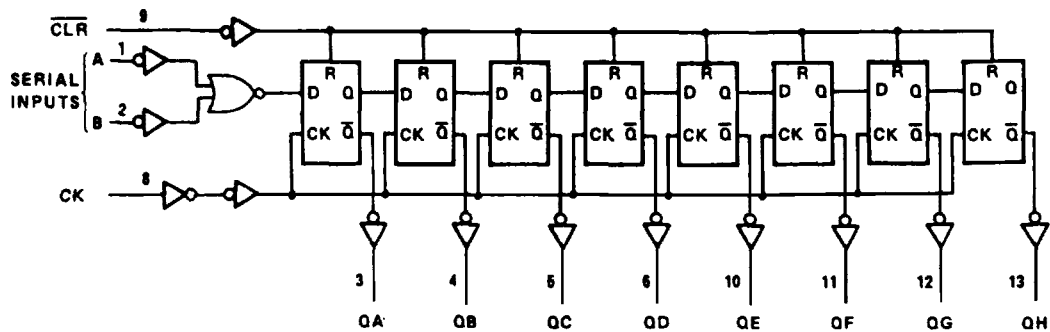
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	$t_{TLH}$ $t_{THL}$	-	-	12	15	ns
Propagation Delay Time (CK-Qn)	$t_{pLH}$ $t_{pHL}$	-	-	20	31	
Propagation Delay Time (CLR--Qn)	$t_{pLH}$ $t_{pHL}$	-	-	20	33	
Maximum Clock Frequency	$f_{MAX}$	-	35	61	-	MHz

AC Electrical Characteristics (C<sub>L</sub> = 50pF, Input  $t_r = t_f = 6\text{ns}$ )

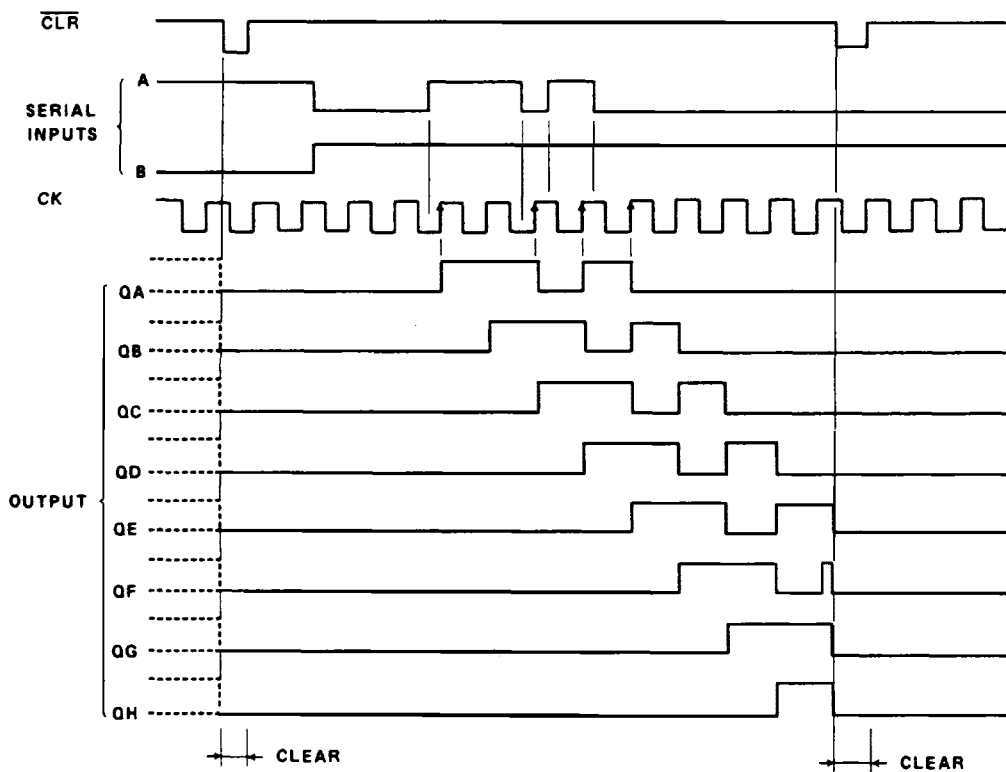
Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit	
			V <sub>CC</sub>	Min.	Typ.	Max.	Min.		Max.
Output Transition Time	$t_{TLH}$ $t_{THL}$	-	4.5	-	8	15	-	19	ns
			5.5	-	7	14	-	18	
Propagation Delay Time (CK-Qn)	$t_{pLH}$ $t_{pHL}$	-	4.5	-	24	36	-	45	
			5.5	-	22	32	-	41	
Propagation Delay Time (CLR--Qn)	$t_{pLH}$ $t_{pHL}$	-	4.5	-	24	38	-	48	
			5.5	-	22	34	-	43	
Maximum Clock Frequency	$f_{MAX}$	-	4.5	30	50	-	24	-	MHz
			5.5	33	60	-	26	-	
Input Capacitance	C <sub>IN</sub>	-	-	5	10	-	10	pF	
Power Dissipation Capacitance	C <sub>PD(1)</sub>	-	-	96	-	-	-		

Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$



Logic Diagram



Timing Chart