8-Bit Shift Register (S-In, P-Out)

The TC74HCT164A is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

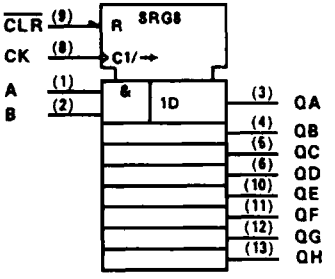
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{CLEAR}$ input. Two serial data inputs (A, B) are provided so that one may be used as a data enable.

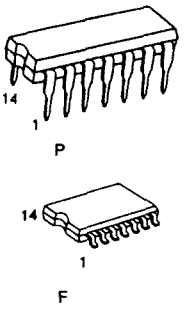
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

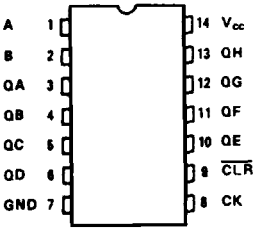
Features:

- High Speed: f_{MAX} = 61MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- Compatible with TTL outputs: V_{IH} = 2V(Min.)
  V_{IL} = 0.8V(Max.)
- Wide Interfacing Ability: LSTTL, NMOS, CMOS
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Pin and Function Compatible with 74LS164



IEC Logic Symbol





(TOP VIEW)

Pin Assignment

Truth Table

Inputs				Outputs			
$\overline{CLR}$	CK	Serial In		QA	QB	--	QH
		A	B				
L	X	X	X	L	L	–	L
H	↓	X	X	No Change			
H	↑	L	X	L	QAn	–	QGn
H	↑	X	L	L	QAn	–	QGn
H	↑	H	H	H	QAn	–	QGn

X: Don't Care

QAn ~ QGn: The level of QA ~ QG, respectively, before the most recent positive edge of the clock.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		4.5 ∫ 5.5	2.0	–	–	2.0	–	V
Low-Level Input Voltage	V_{IL}	–		4.5 ∫ 5.5	–	–	0.8	–	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	4.5	4.5	4.5	–	4.4	–	V
			I_{OH} = -4 mA	4.5	4.18	4.31	–	4.13	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	4.5	–	0.0	0.1	–	0.1	V
			I_{OL} = 4mA	4.5	–	0.17	0.26	–	0.33	
Input Leakage Current	i_{IN}	V_{IN} = V_{CC} or GND		5.5	–	–	±0.1	–	±0.1	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	–	–	4.0	–	40.0	μA
	ΔI_{CC}	Per Input: V_{IN} = 0.5V or 2.4V Other Input: V_{CC} or GND		5.5	–	–	2.0	–	2.9	mA

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	–	4.5 5.5	– –	15 14	19 18	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(H)}$	–	4.5 5.5	– –	15 14	19 18	
Minimum Set-up Time (A, B)	t_s	–	4.5 5.5	– –	10 9	13 11	
Minimum Hold Time (A,B)	t_h	–	4.5 5.5	– –	0 0	0 0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	–	4.5 5.5	– –	10 9	13 11	
Clock Frequency	f	–	4.5 5.5	– –	30 33	24 26	MHz

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

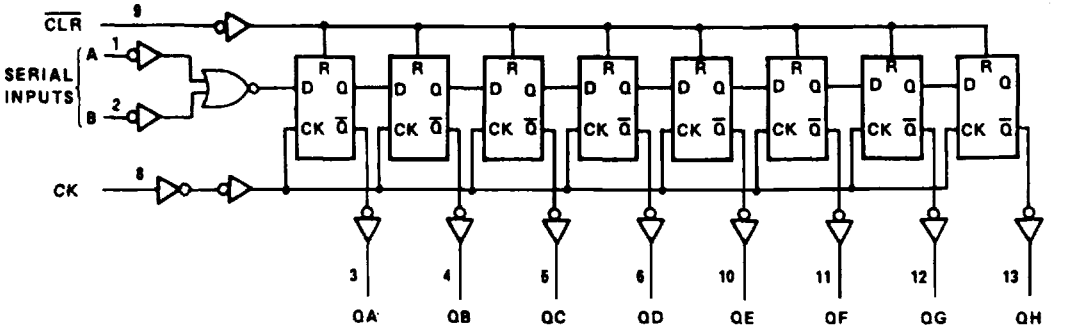
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	12	15	ns
Propagation Delay Time (CK-Qn)	t_{pLH} t_{pHL}	–	–	20	31	
Propagation Delay Time ($\overline{CLR}$--Qn)	t_{pLH} t_{pHL}	–	–	20	33	
Maximum Clock Frequency	f_{MAX}	–	35	61	–	MHz

AC Electrical Characteristics ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

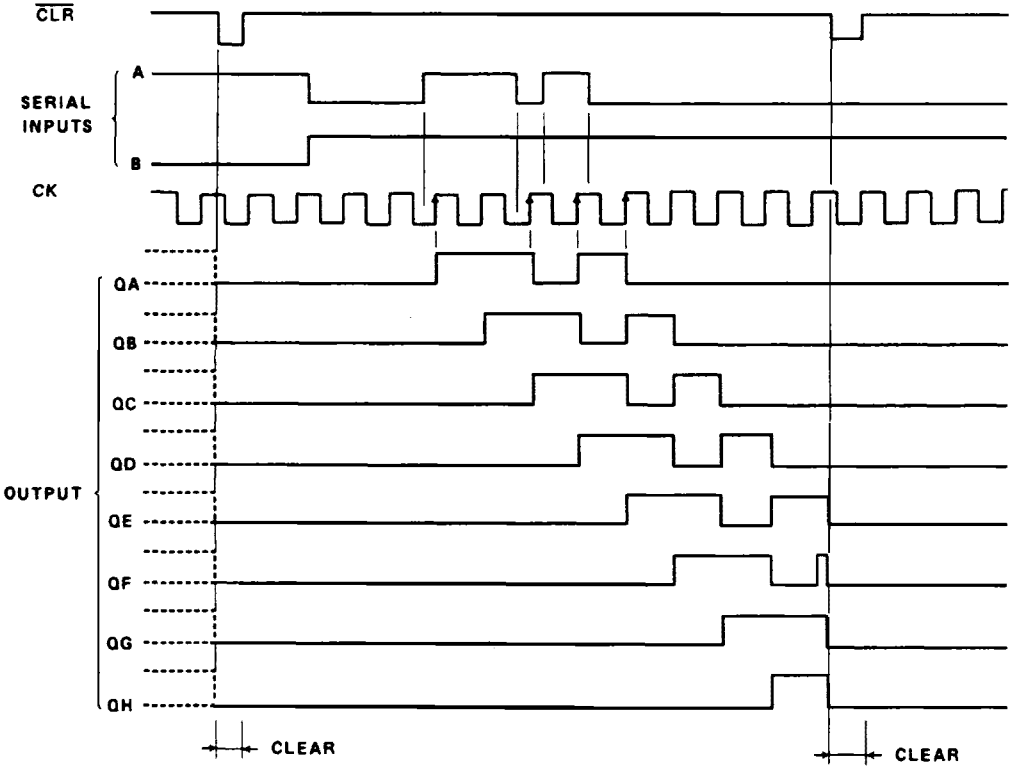
Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time (CK-Qn)	t_{pLH} t_{pHL}	–	4.5 5.5	– –	24 22	36 32	– –	45 41	
Propagation Delay Time ($\overline{CLR}$--Qn)	t_{pLH} t_{pHL}	–	4.5 5.5	– –	24 22	38 34	– –	48 43	
Maximum Clock Frequency	f_{MAX}	–	4.5 5.5	30 33	50 60	– –	24 26	– –	MHz
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	–		–	96	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$



Logic Diagram



Timing Chart