

HD74HC173

4-bit D-type Register (with 3-state outputs)

REJ03D0583-0200
(Previous ADE-205-459)
Rev.2.00
Oct 11, 2005

Description

The four D type Flip-Flops operate synchronously from a common clock. The 3-state outputs allow the device to be used in bus organized systems. The outputs are placed in the 3-stage mode when either of the output disable pins are in the logic high level.

The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic high level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Clearing is enabled by taking the clear input to a logic high level. The data outputs change state on the positive going edge of the clock.





Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---------------|--------------------|------------------------------|----------------------|--------------------------------|
| HD74HC173P | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74HC173FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |
| HD74HC173RPEL | SOP-16 pin (JEDEC) | PRSP0016DG-A (FP-16DNV) | RP | EL (2,500 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Function Table

| Inputs | | | | | Output Q |
|--------|---|----------------|----------------|--------|----------------|
| Clear | Clock | Data Enable | | Data D | |
| | | G ₁ | G ₂ | | |
| H | X | X | X | X | L |
| L | L | X | X | X | Q ₀ |
| L |  | H | X | X | Q ₀ |
| L |  | X | H | X | Q ₀ |
| L |  | L | L | L | L |
| L |  | L | L | H | H |

Note: When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

Q_{A0} to Q_{H0} = Outputs remain unchanged.

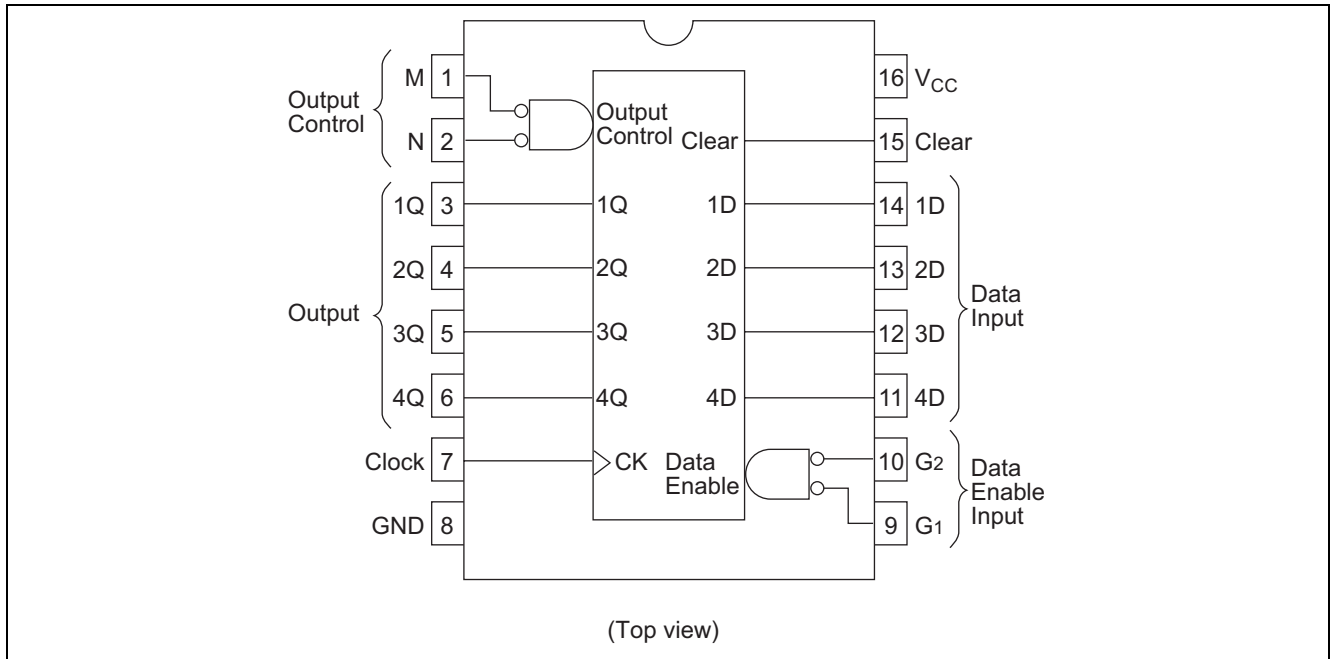
Q_{An} to Q_{Gn} = Data shifted from the previous stage on a positive edge at the clock input.

H : High level

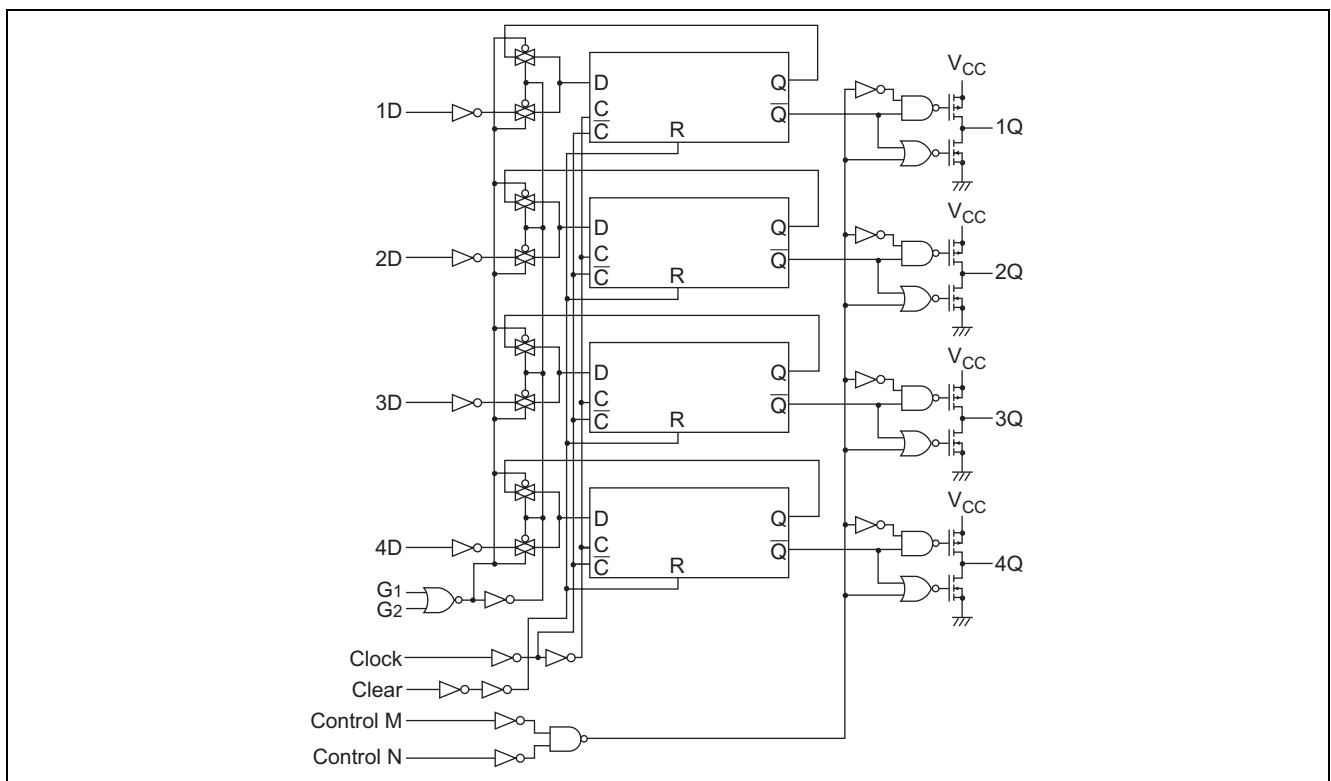
L : Low level

X : Irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|------------------------------|-----------------------|------------------------|------|
| Supply voltage range | V_{CC} | -0.5 to 7.0 | V |
| Input / Output voltage | V_{in}, V_{out} | -0.5 to $V_{CC} + 0.5$ | V |
| Input / Output diode current | I_{IK}, I_{OK} | ± 20 | mA |
| Output current | I_O | ± 35 | mA |
| V_{CC} , GND current | I_{CC} or I_{GND} | ± 75 | mA |
| Power dissipation | P_T | 500 | mW |
| Storage temperature | T_{stg} | -65 to +150 | °C |

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

| Item | Symbol | Ratings | Unit | Conditions |
|--------------------------------------|-------------------|----------------|------|------------------|
| Supply voltage | V_{CC} | 2 to 6 | V | |
| Input / Output voltage | V_{IN}, V_{OUT} | 0 to V_{CC} | V | |
| Operating temperature | T_a | -40 to 85 | °C | |
| Input rise / fall time ^{*1} | t_r, t_f | 0 to unlimited | ns | $V_{CC} = 2.0$ V |
| | | 0 to unlimited | | $V_{CC} = 4.5$ V |
| | | 0 to unlimited | | $V_{CC} = 6.0$ V |

Note: 1. This item guarantees maximum limit when one input switches.

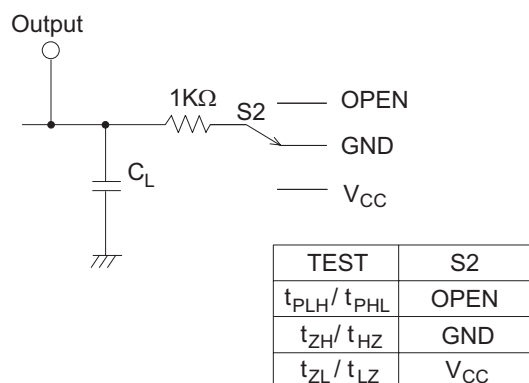
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

| Item | Symbol | V _{CC} (V) | Ta = 25°C | | | Ta = -40 to+85°C | | Unit | Test Conditions | |
|--------------------------|-----------------|---------------------|-----------|-----|------|------------------|------|------|---|---------------------------|
| | | | Min | Typ | Max | Min | Max | | | |
| Input voltage | V _{IH} | 2.0 | 1.5 | — | — | 1.5 | — | V | | |
| | | 4.5 | 3.15 | — | — | 3.15 | — | | | |
| | | 6.0 | 4.2 | — | — | 4.2 | — | | | |
| | V _{IL} | 2.0 | — | — | 0.5 | — | 0.5 | V | | |
| | | 4.5 | — | — | 1.35 | — | 1.35 | | | |
| | | 6.0 | — | — | 1.8 | — | 1.8 | | | |
| Output voltage | V _{OH} | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V | Vin = V _{IH} or V _{IL} | I _{OH} = -20 μA |
| | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | | | I _{OH} = -6 mA |
| | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | | | I _{OH} = -7.8 mA |
| | | 4.5 | 4.18 | — | — | 4.13 | — | | | |
| | | 6.0 | 5.68 | — | — | 5.63 | — | | | |
| | V _{OL} | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V | Vin = V _{IH} or V _{IL} | I _{OL} = 20 μA |
| | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 4.5 | — | — | 0.26 | — | 0.33 | | | I _{OL} = 6 mA |
| | | 6.0 | — | — | 0.26 | — | 0.33 | | | I _{OL} = 7.8 mA |
| Off-state output current | I _{OZ} | 6.0 | — | — | ±0.5 | — | ±5.0 | μA | Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND | |
| Input current | I _{in} | 6.0 | — | — | ±0.1 | — | ±1.0 | μA | Vin = V _{CC} or GND | |
| Quiescent supply current | I _{CC} | 6.0 | — | — | 4.0 | — | 40 | μA | Vin = V _{CC} or GND, Iout = 0 μA | |

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

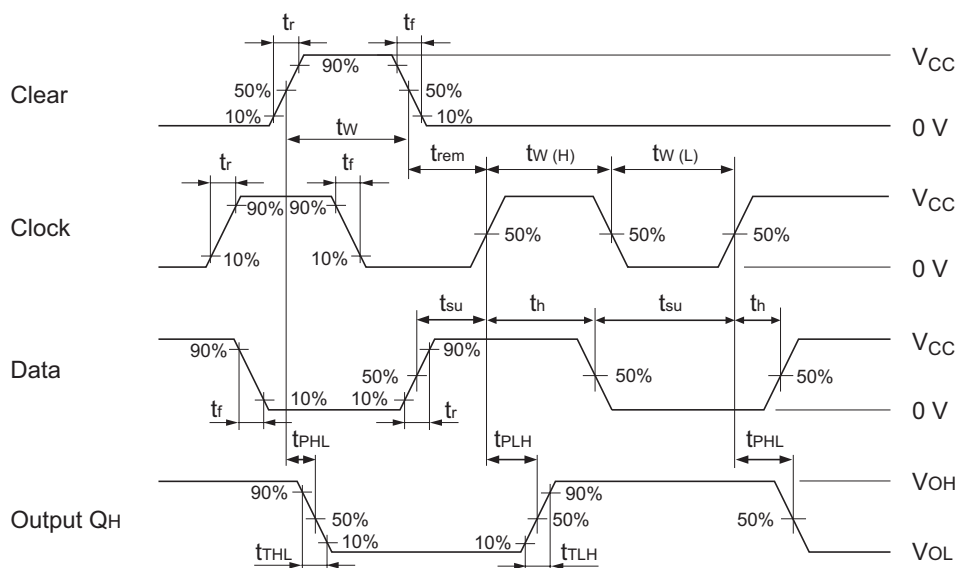
| Item | Symbol | $V_{CC} \text{ (V)}$ | $T_a = 25^\circ\text{C}$ | | | $T_a = -40 \text{ to } +85^\circ\text{C}$ | | Unit | Test Conditions |
|-------------------------|--------------------|----------------------|--------------------------|-----|-----|---|-----|------|-----------------|
| | | | Min | Typ | Max | Min | Max | | |
| Maximum clock frequency | f_{\max} | 2.0 | — | — | 5 | — | 4 | MHz | |
| | | 4.5 | — | — | 27 | — | 21 | | |
| | | 6.0 | — | — | 32 | — | 25 | | |
| Propagation delay time | t_{PLH}, t_{PHL} | 2.0 | — | — | 175 | — | 220 | ns | Clock to Q |
| | | 4.5 | — | 14 | 35 | — | 44 | | |
| | | 6.0 | — | — | 30 | — | 37 | | |
| | t_{PHL} | 2.0 | — | — | 150 | — | 190 | ns | Clear to Q |
| | | 4.5 | — | 14 | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| Enable time | t_{ZH}, t_{ZL} | 2.0 | — | — | 150 | — | 190 | ns | |
| | | 4.5 | — | 12 | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| Disable time | t_{HZ}, t_{LZ} | 2.0 | — | — | 150 | — | 190 | ns | |
| | | 4.5 | — | 12 | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| Setup time | t_{su} | 2.0 | 100 | — | — | 125 | — | ns | |
| | | 4.5 | 20 | 4 | — | 25 | — | | |
| | | 6.0 | 17 | — | — | 21 | — | | |
| Removal time | t_{rem} | 2.0 | 90 | — | — | 115 | — | ns | |
| | | 4.5 | 18 | 0 | — | 23 | — | | |
| | | 6.0 | 15 | — | — | 20 | — | | |
| Hold time | t_h | 2.0 | 5 | — | — | 5 | — | ns | |
| | | 4.5 | 5 | -2 | — | 5 | — | | |
| | | 6.0 | 5 | — | — | 5 | — | | |
| Pulse width | t_w | 2.0 | 80 | — | — | 100 | — | ns | |
| | | 4.5 | 16 | 4 | — | 20 | — | | |
| | | 6.0 | 14 | — | — | 17 | — | | |
| Output rise/fall time | t_{TLH}, t_{THL} | 2.0 | — | — | 60 | — | 75 | ns | |
| | | 4.5 | — | 4 | 12 | — | 15 | | |
| | | 6.0 | — | — | 10 | — | 13 | | |
| Input capacitance | C_{in} | — | — | 5 | 10 | — | 10 | pF | |

Test Circuit

Note 1. C_L includes probe and jig capacitance

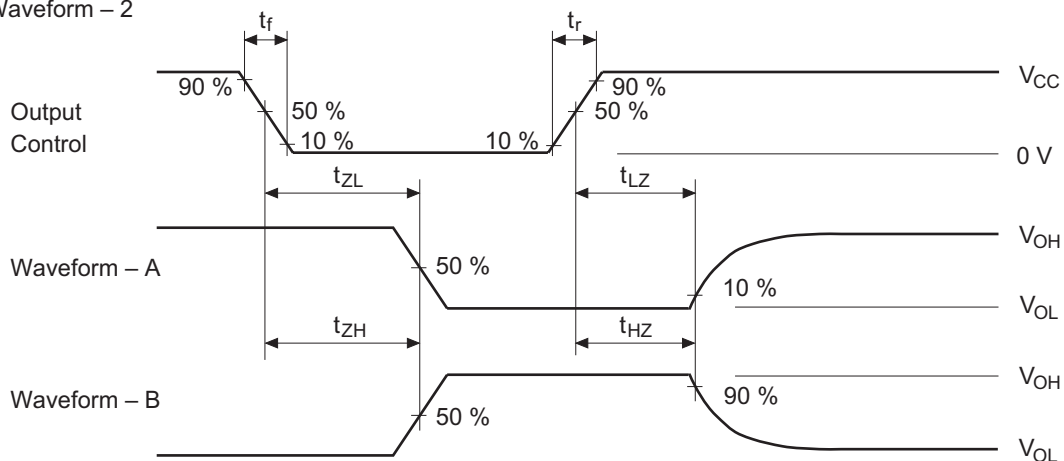
Waveforms

• Waveform – 1



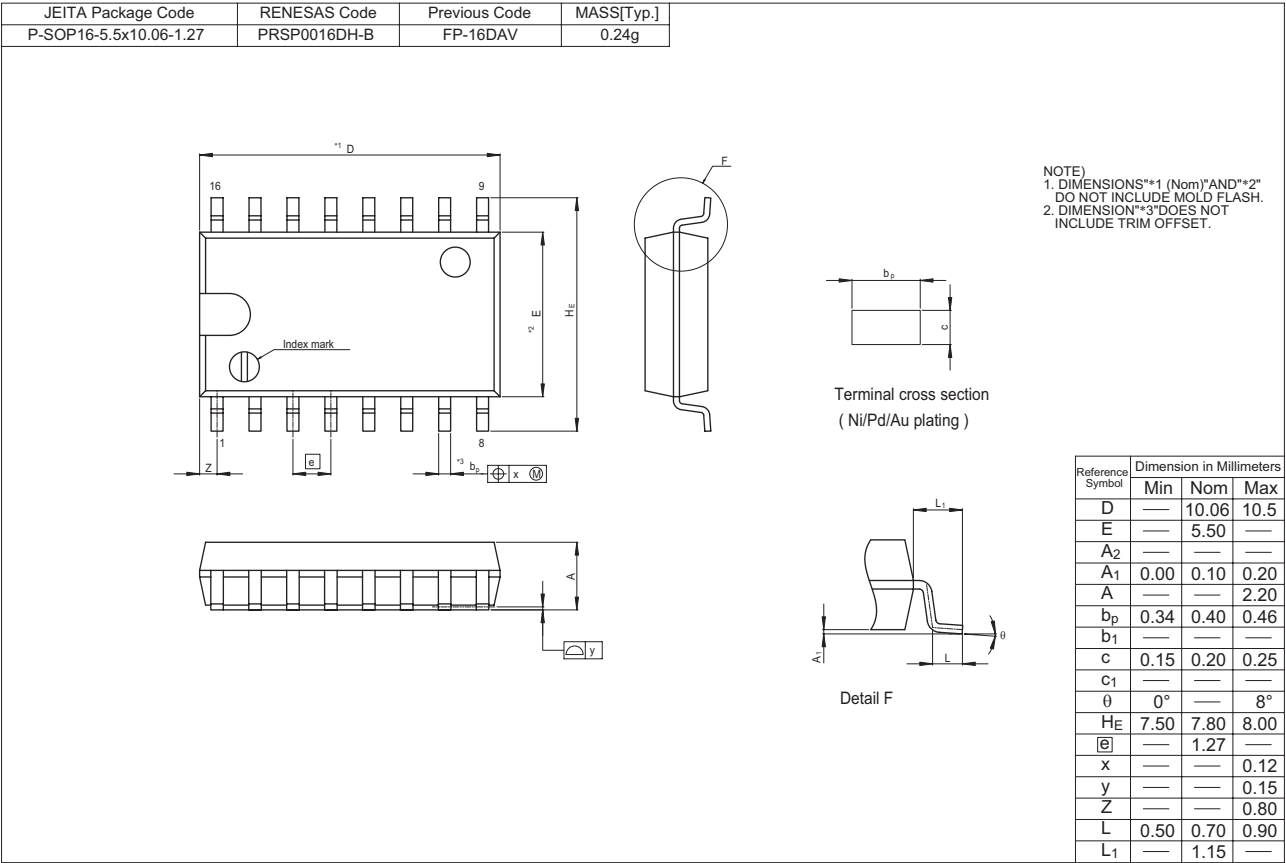
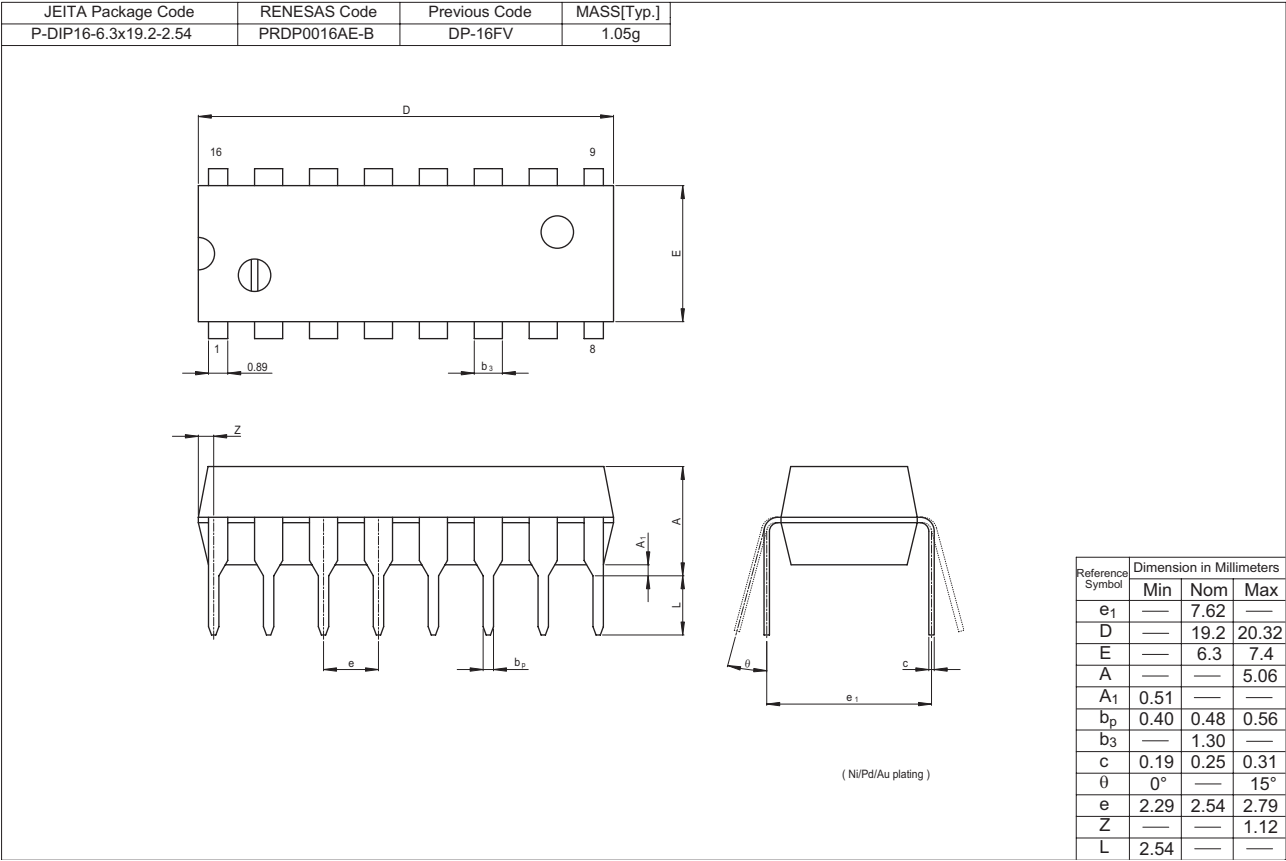
Note 1. Input pulse : $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$

• Waveform – 2

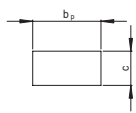
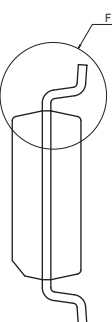
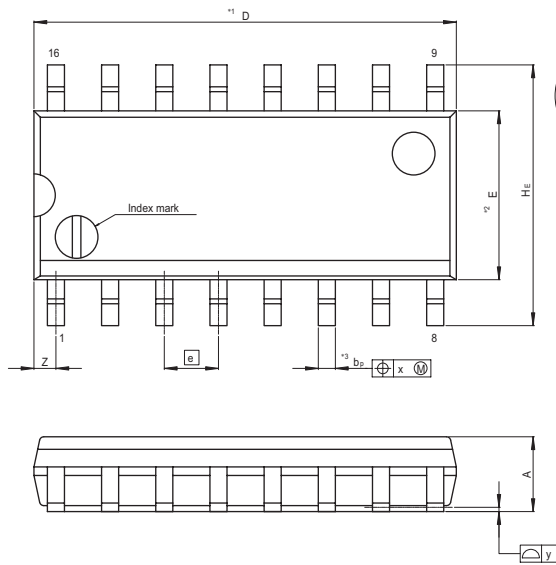


- Notes 1. Input pulse $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

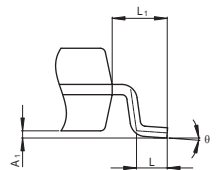
Package Dimensions



| | | | |
|-----------------------|--------------|---------------|------------|
| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
| P-SOP16-3.95x9.9-1.27 | PRSP0016DG-A | FP-16DNV | 0.15g |



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|---------------------|--------------------------|------|-------|
| | Min | Nom | Max |
| D | — | 9.90 | 10.30 |
| E | — | 3.95 | — |
| A ₂ | — | — | — |
| A ₁ | 0.10 | 0.14 | 0.25 |
| A | — | — | 1.75 |
| b _p | 0.34 | 0.40 | 0.46 |
| b ₁ | — | — | — |
| c | 0.15 | 0.20 | 0.25 |
| c ₁ | — | — | — |
| θ | 0° | — | 8° |
| H _E | 5.80 | 6.10 | 6.20 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.15 |
| Z | — | — | 0.635 |
| L | 0.40 | 0.60 | 1.27 |
| L ₁ | — | 1.08 | — |

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