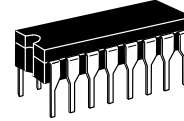


**CMOS MSI**  
**Quad R–S Latches**

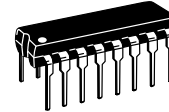
The MC14043B and MC14044B quad R–S latches are constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc

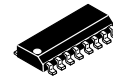
**MC14043B**  
**MC14044B**



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648

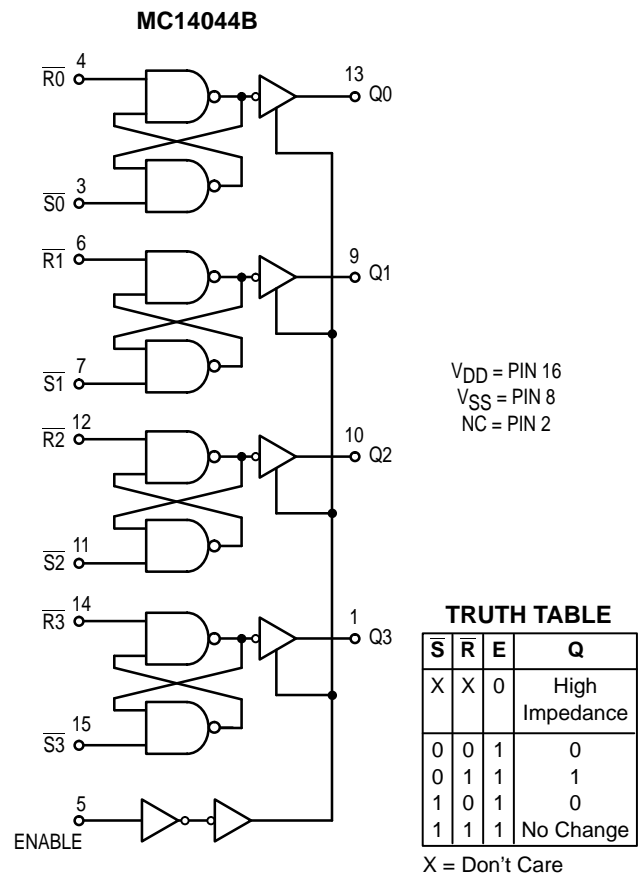
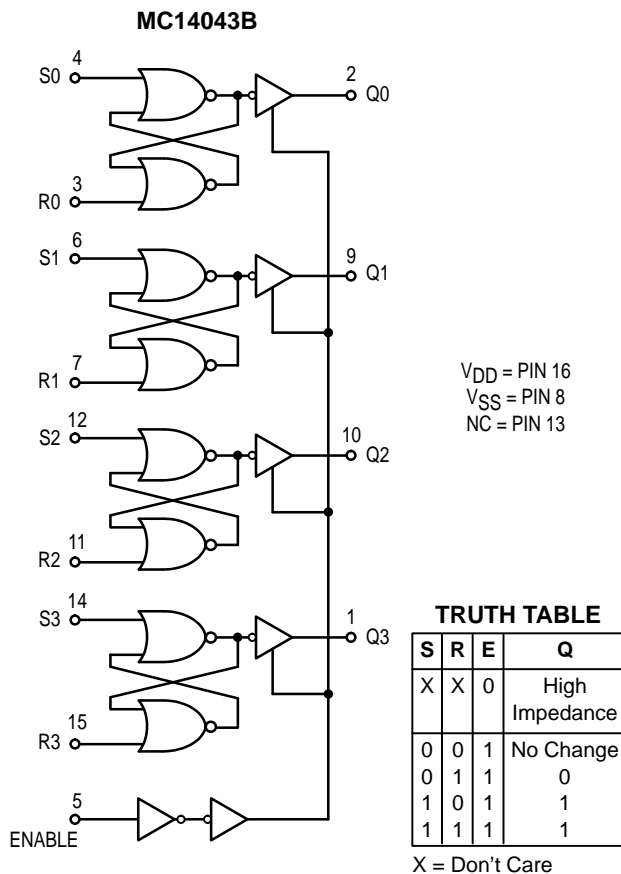


**D SUFFIX**  
SOIC  
CASE 751B

**ORDERING INFORMATION**

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

T<sub>A</sub> = – 55° to 125°C for all packages.



**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	“0” Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
	“1” Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage V <sub>O</sub> = 4.5 or 0.5 Vdc V <sub>O</sub> = 9.0 or 1.0 Vdc V <sub>O</sub> = 13.5 or 1.5 Vdc  V <sub>O</sub> = 0.5 or 4.5 Vdc V <sub>O</sub> = 1.0 or 9.0 Vdc V <sub>O</sub> = 1.5 or 13.5 Vdc	“0” Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
	“1” Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current V <sub>OH</sub> = 2.5 Vdc V <sub>OH</sub> = 4.6 Vdc V <sub>OH</sub> = 9.5 Vdc V <sub>OH</sub> = 13.5 Vdc  V <sub>OL</sub> = 0.4 Vdc V <sub>OL</sub> = 0.5 Vdc V <sub>OL</sub> = 1.5 Vdc	Source I <sub>OH</sub>	5.0	- 3.0	—	- 2.4	- 4.2	—	- 1.7	—	mAdc
		5.0	- 0.64	—	- 0.51	- 0.88	—	- 0.36	—	
		10	- 1.6	—	- 1.3	- 2.25	—	- 0.9	—	
		15	- 4.2	—	- 3.4	- 8.8	—	- 2.4	—	
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15		4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	1.0	—	0.002	1.0	—	30	µAdc
		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.58 µA/kHz) f + I <sub>DD</sub>							µAdc
		10	I <sub>T</sub> = (1.15 µA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (1.73 µA/kHz) f + I <sub>DD</sub>							
Three-State Output Leakage Current	I <sub>TL</sub>	15	—	± 0.1	—	± 0.0001	± 0.1	—	± 3.0	µAdc

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in µA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.004.

\* Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating: Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C  
Ceramic “L” Packages - 12 mW/°C From 100°C To 125°C

**MAXIMUM RATINGS\*** (Voltages Referenced to  $V_{SS}$ )

Symbol	Parameter	Value	Unit
$V_{DD}$	DC Supply Voltage	- 0.5 to + 18.0	V
$V_{in}, V_{out}$	Input or Output Voltage (DC or Transient)	- 0.5 to $V_{DD} + 0.5$	V
$I_{in}, I_{out}$	Input or Output Current (DC or Transient), per Pin	$\pm 10$	mA
$P_D$	Power Dissipation, per Package†	500	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.

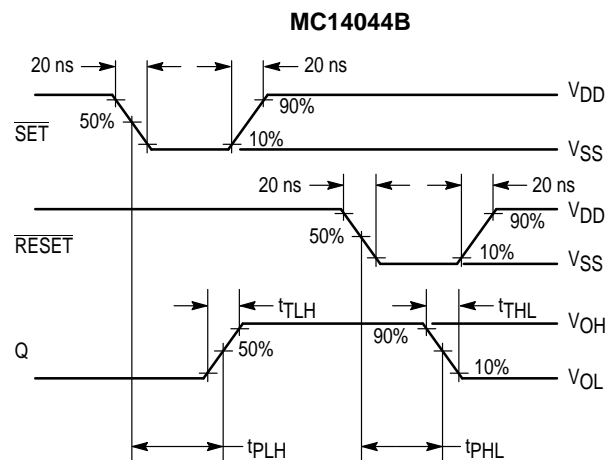
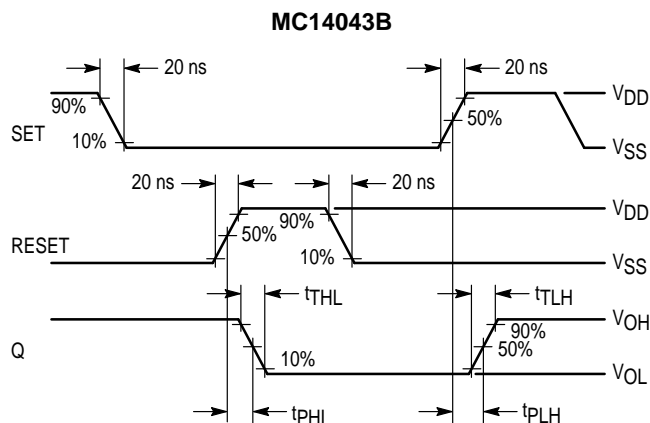
**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}, T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ #	Max	Unit
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{TLH}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 32.5 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	$t_{THL}$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time $t_{PLH} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PLH} = (0.36 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 130 \text{ ns}$ $t_{PHL} = (0.90 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PHL} = (0.26 \text{ ns/pF}) C_L + 47 \text{ ns}$	$t_{PLH}$	5.0	—	175	350	ns
		10	—	75	175	
		15	—	60	120	
	$t_{PHL}$	5.0	—	175	350	ns
		10	—	75	175	
		15	—	60	120	
Set, $\overline{\text{Set}}$ Pulse Width	$t_W$	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Reset, $\overline{\text{Reset}}$ Pulse Width	$t_W$	5.0	200	80	—	ns
		10	100	40	—	
		15	70	30	—	
Three-State Enable/Disable Delay	$t_{PLZ},$	5.0	—	150	300	ns
	$t_{PHZ},$	10	—	80	160	
	$t_{PZL},$	15	—	55	110	
	$t_{PZH}$					

\* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

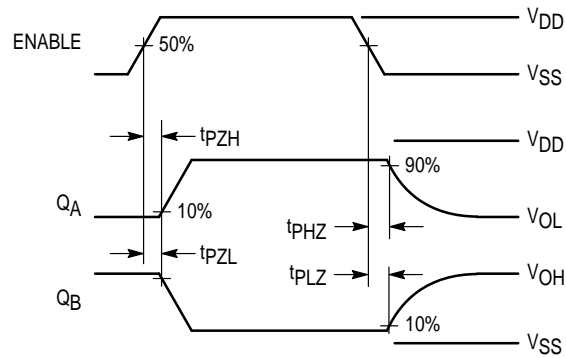
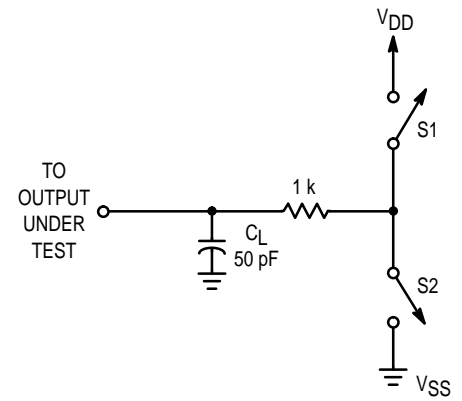
**AC WAVEFORMS**



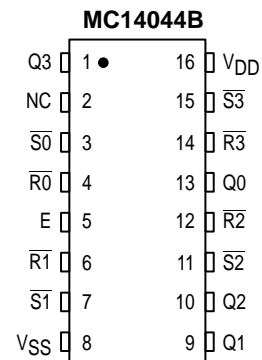
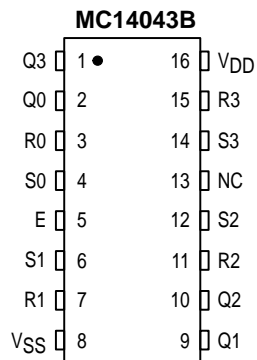
### THREE-STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3-State Tests

Test	Enable	S1	S2	Q	MC14043B		MC14044B	
					S	R	$\bar{S}$	$\bar{R}$
tPZH	✓	Open	Closed	A	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>
tPZL	✓	Closed	Open	B	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>SS</sub>
tPHZ	↘	Open	Closed	A	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>
tPLZ	↘	Closed	Open	B	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DD</sub>	V <sub>SS</sub>



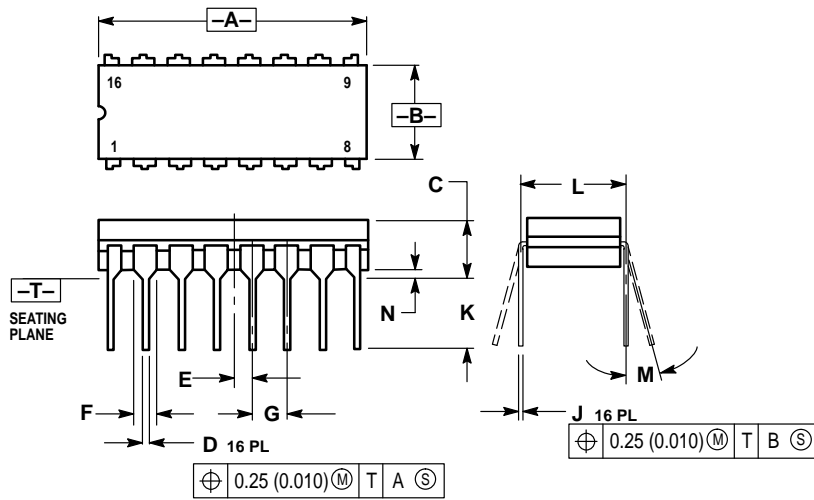
### PIN ASSIGNMENT



NC = NO CONNECTION

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



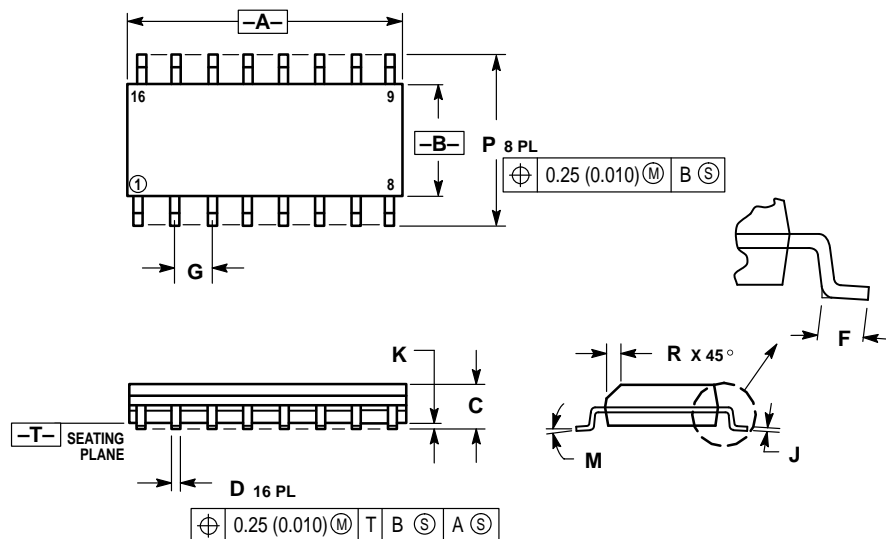
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

**How to reach us:**

**USA/EUROPE/Locations Not Listed:** Motorola Literature Distribution;  
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center,  
3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

**MFAX:** RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609  
**INTERNET:** http://Design-NET.com

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



MC14043B/D

