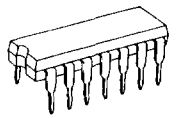
TC4011BP/BF/BFN, TC4012BP/BF TC4023BP/BF/BFN

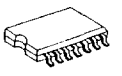
TC4011B QUAD 2 INPUT NAND GATE
TC4012B DUAL 4 INPUT NAND GATE
TC4023B TRIPLE 3 INPUT NAND GATE

The TC4011B, TC4023B, and TC4012B are 2-input, 3-input, and 4-input positive logic NAND gates respectively.

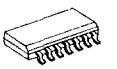
Since all the outputs of these gates are provided with the inverters as buffers, the input / output characteristics have been improved and the variation of propagation delay time due to the increase in load capacity is kept down to the minimum.



P (DIP14-P-300)



F (SOP14-P-300)



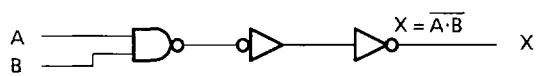
FN (SOL14-P-150)

ABSOLUTE MAXIMUM RATINGS

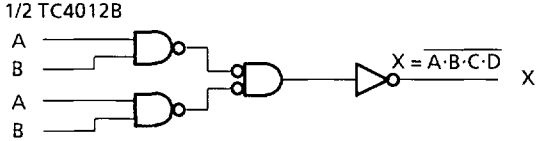
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) /180 (SOIC)	mW
Operating Temperature Range	T_A	−40~85	°C
Storage Temperature Range	T_{STG}	−65~150	°C
Lead Temp./Time	T_{SOL}	260°C · 10sec	

LOGIC DIAGRAM

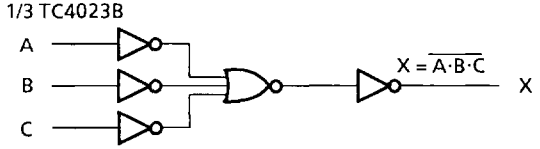
1/4 TC4011B



1/2 TC4012B

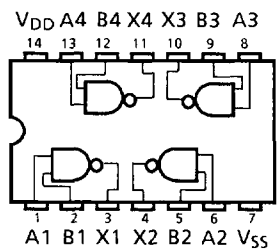


1/3 TC4023B

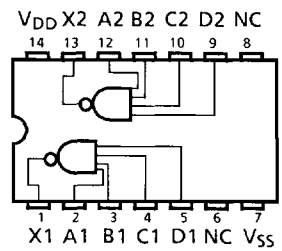


PIN ASSIGNMENT (TOP VIEW)

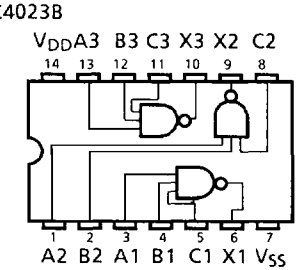
TC4011B



TC4012B



TC4023B



RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTICS	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	–	18	V
Input Voltage	V_{IN}		0	–	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTICS		SYMBOL	TEST CONDITIONS	V_{DD} (V)	−40°C		25°C			85°C		UNITS
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	4.95 9.95 14.95	– – –	4.95 9.95 14.95	5.00 10.00 15.00	– – –	4.95 9.95 14.95	– – –	V
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\| < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5 10 15	– – –	0.05 0.05 0.05	– – –	0.00 0.00 0.00	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
Output High Current		I_{OH}	V_{OH} = 4.6V V_{OH} = 2.5V V_{OH} = 9.5V V_{OH} = 13.5V $V_{IN} = V_{SS}, V_{DD}$	5 5 10 15	−0.61 −2.5 −1.5 −4.0	– – – –	−0.51 −2.1 −1.3 −3.4	−1.0 −4.0 −2.2 −9.0	– – – –	−0.42 −1.7 −1.1 −2.8	– – – –	mA
Output Low Current		I_{OL}	V_{OL} = 0.4V V_{OL} = 0.5V V_{OL} = 1.5V $V_{IN} = V_{SS}, V_{DD}$	5 10 15	0.61 1.5 4.0	– – –	0.51 1.3 3.4	1.2 3.2 12.0	– – –	0.42 1.1 2.8	– – –	mA
Input High Voltage		V_{IH}	V_{OUT} = 0.5V V_{OUT} = 1.0V V_{OUT} = 1.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	3.5 7.0 11.0	– – –	3.5 7.0 11.0	2.75 5.5 8.25	– – –	3.5 7.0 11.0	– – –	V
Input Low Voltage		V_{IL}	V_{OUT} = 4.5V V_{OUT} = 9.0V V_{OUT} = 13.5V $\|I_{OUT}\| < 1\mu A$	5 10 15	– – –	1.5 3.0 4.0	– – –	2.25 4.5 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
Input Current	"H" Level	I_{IH}	V_{IH} = 18V	18	–	0.1	–	10^{-5}	0.1	–	1.0	μA
	"L" Level	I_{IL}	V_{IL} = 0V	18	–	−0.1	–	-10^{-5}	−0.1	–	−1.0	μA
Quiescent Device Current		I_{DD}	$V_{IN} = V_{SS}, V_{DD}$*	5 10 15	– – –	0.25 0.5 1.0	– – –	0.001 0.001 0.002	0.25 0.5 1.0	– – –	7.5 15 30	μA

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{SS} = 0V, C_L = 50pF)

CHARACTERISTICS	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNITS
Output Transition Time (TC4012B)	t_{TLH}		5	–	80	200	ns
			10	–	50	100	
			15	–	40	80	
Output Transition Time (TC4012B)	t_{THL}		5	–	80	200	
			10	–	50	100	
			15	–	40	80	
Output Transition Time (TC4011B, TC4023B)	t_{TLH}		5	–	70	200	
			10	–	35	100	
			15	–	30	80	
Output Transition Time (TC4011B, TC4023B)	t_{THL}		5	–	70	200	
			10	–	35	100	
			15	–	30	80	
Propagation Delay Time (TC4011B)	t_{pLH}		5	–	65	200	
			10	–	30	100	
			15	–	25	80	
Propagation Delay Time (TC4011B)	t_{pHL}		5	–	65	200	
			10	–	30	100	
			15	–	25	80	
Propagation Delay Time (TC4012B)	t_{pLH}		5	–	95	250	
			10	–	45	120	
			15	–	30	90	
Propagation Delay Time (TC4012B)	t_{pHL}		5	–	95	250	
			10	–	45	120	
			15	–	30	90	
Propagation Delay Time (TC4023B)	t_{pLH}		5	–	90	250	
			10	–	45	100	
			15	–	35	80	
Propagation Delay Time (TC4023B)	t_{pHL}		5	–	90	250	
			10	–	45	100	
			15	–	35	80	
Input Capacitance	C_{IN}			–	5	7.5	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS