MC14008B

4-Bit Full Adder

The MC14008B 4–bit full adder is constructed with MOS P–channel and N–channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look–ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high–speed operation when used with other adders in a system.

- Look–Ahead Carry Output
- Diode Protection on All Inputs
- All Outputs Buffered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4008B

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP   Plastic
MC14XXXBCL   Ceramic
MC14XXXBD   SOIC

$T_A = -55°$ to $125°C$ for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

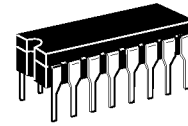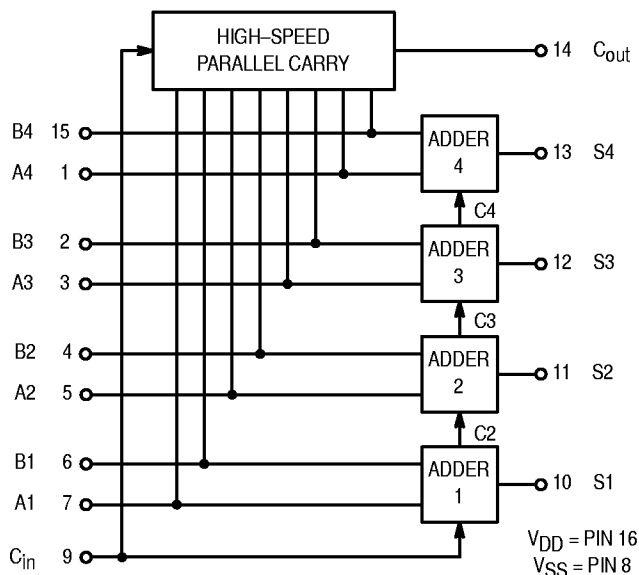| Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
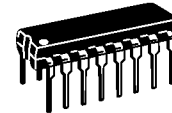†Temperature Derating:
     Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C
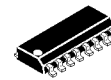   Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C

TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

BLOCK DIAGRAM

PIN ASSIGNMENT

A4	1 ●	16	V_{DD}
B3	2	15	B4
A3	3	14	C_{out}
B2	4	13	S4
A2	5	12	S3
B1	6	11	S2
A1	7	10	S1
V_{SS}	8	9	C_{in}

MOTOROLA
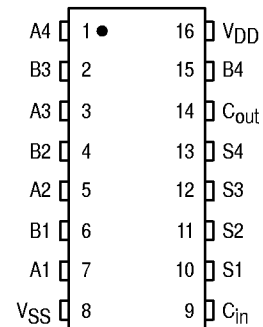
ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
		15	—	4.0	—	6.75	4.0	—	4.0	
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
		15	11	—	11	8.25	—	11	—	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	mAdc
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0			I_T = (1.7 μA/kHz) f + I_{DD}					μAdc
		10			I_T = (3.4 μA/kHz) f + I_{DD}					
		15			I_T = (5.0 μA/kHz) f + I_{DD}					

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH},					ns
$\quad t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) \, C_L + 25 \text{ ns}$	t_{THL}	5.0	—	100	200	
$\quad t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) \, C_L + 12.5 \text{ ns}$		10	—	50	100	
$\quad t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) \, C_L + 9.5 \text{ ns}$		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
$\quad$ Sum in to Sum Out						
$\qquad t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \, C_L + 315 \text{ ns}$		5.0	—	400	800	
$\qquad t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \, C_L + 127 \text{ ns}$		10	—	160	320	
$\qquad t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \, C_L + 90 \text{ ns}$		15	—	115	230	
$\quad$ Sum In to Carry Out						
$\qquad t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \, C_L + 220 \text{ ns}$		5.0	—	305	610	
$\qquad t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \, C_L + 112 \text{ ns}$		10	—	145	290	
$\qquad t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \, C_L + 85 \text{ ns}$		15	—	110	220	
$\quad$ Carry In to Sum Out						
$\qquad t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \, C_L + 290 \text{ ns}$		5.0	—	375	750	
$\qquad t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \, C_L + 122 \text{ ns}$		10	—	155	310	
$\qquad t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \, C_L + 90 \text{ ns}$		15	—	115	230	
$\quad$ Carry In to Carry Out						
$\qquad t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) \, C_L + 85 \text{ ns}$		5.0	—	170	340	
$\qquad t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) \, C_L + 42 \text{ ns}$		10	—	75	150	
$\qquad t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) \, C_L + 30 \text{ ns}$		15	—	55	110	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
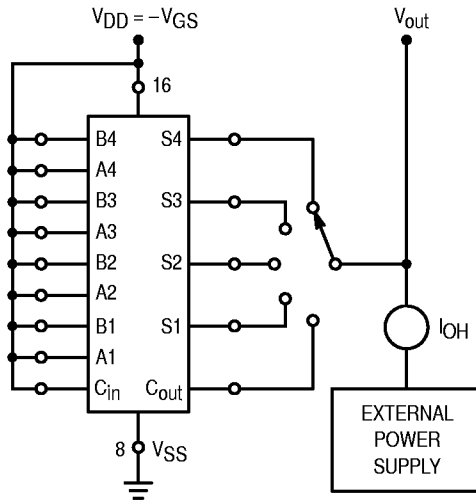

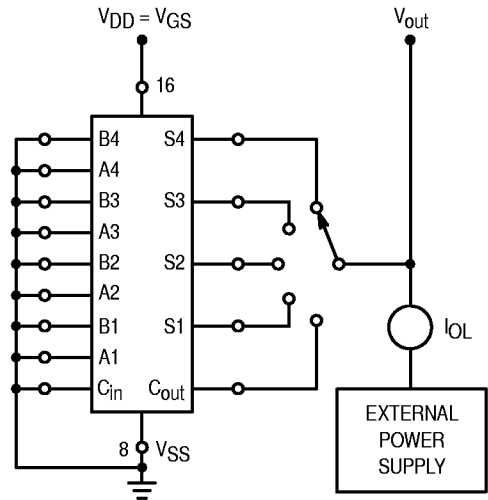**Figure 1. Typical Source Current
Characteristics Test Circuit**

**Figure 2. Typical Sink Current
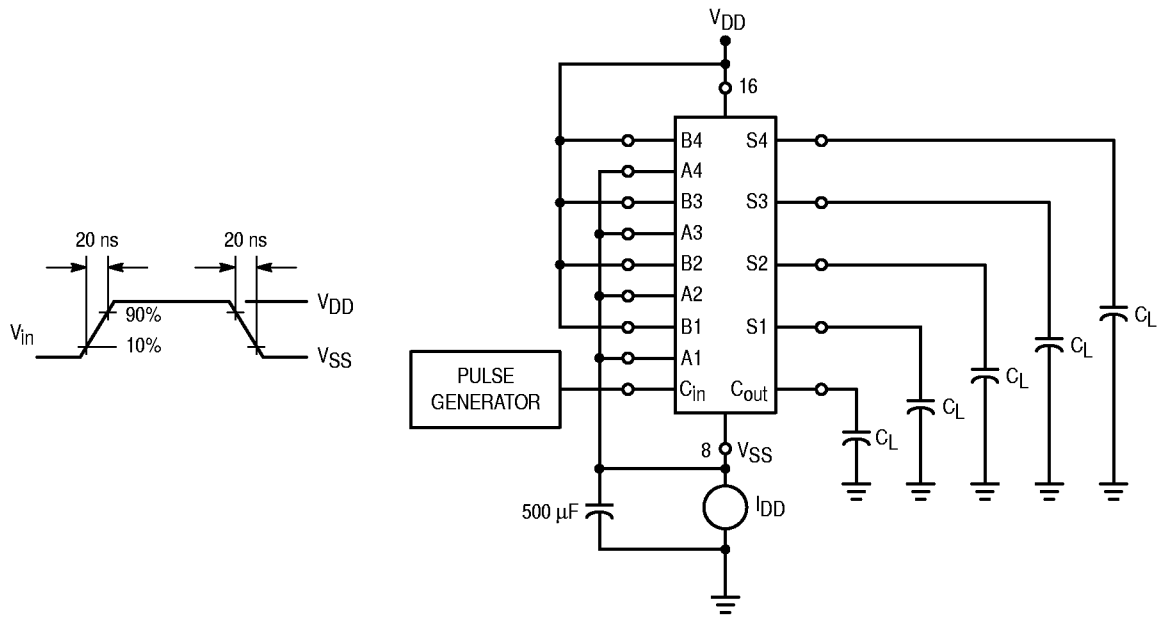Characteristics Test Circuit**

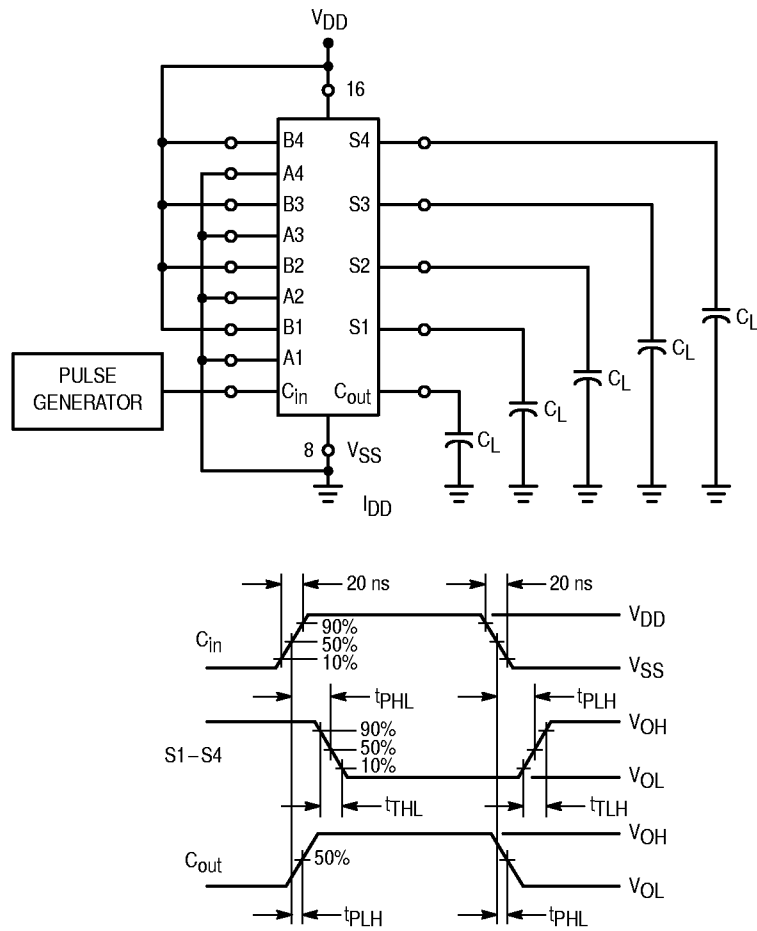**Figure 3. Dynamic Power Dissipation Test Circuit and Waveform**

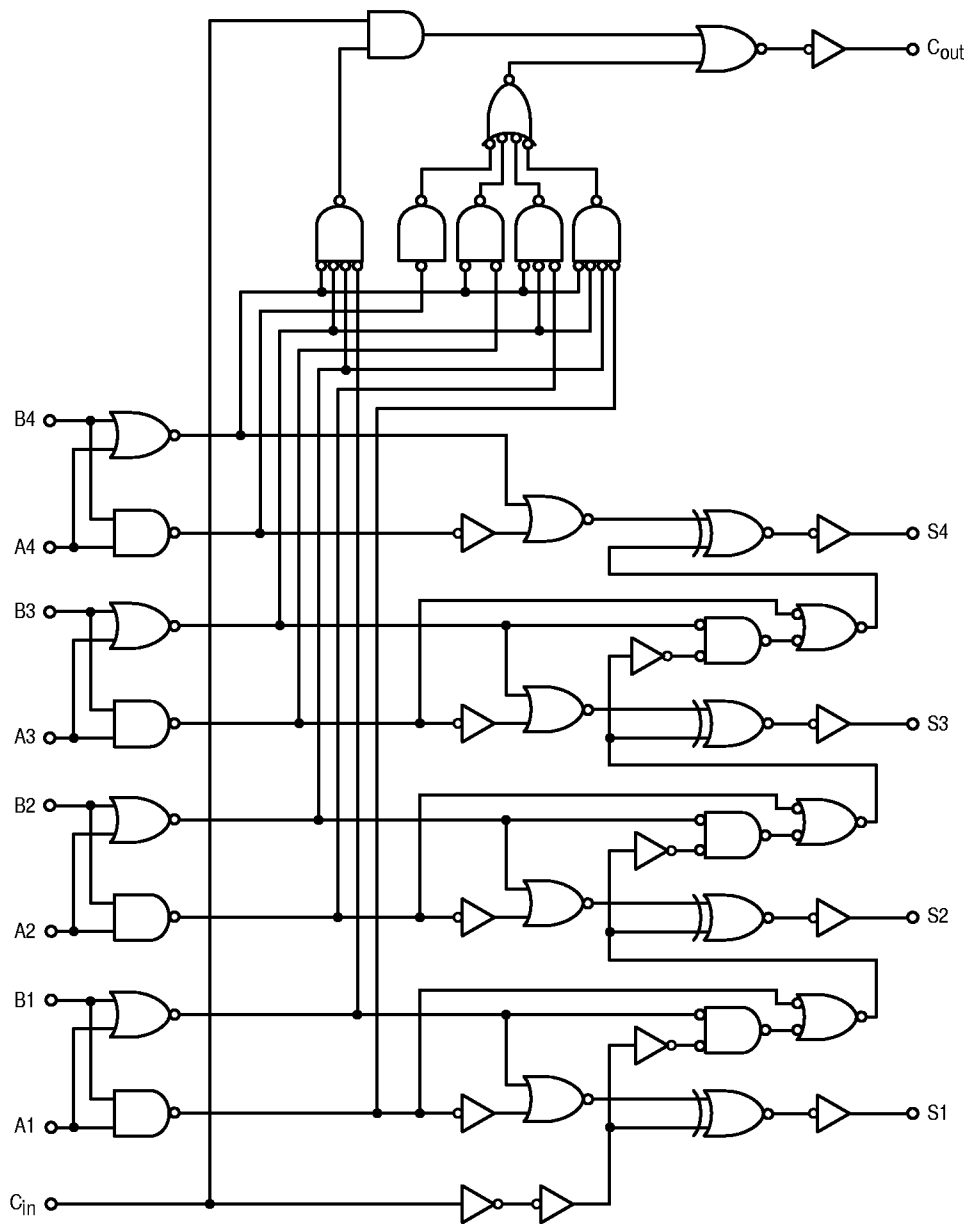**Figure 4. Switching Time Test Circuit and Waveforms**

Figure 5. Logic Diagram

TYPICAL APPLICATION

WORD A + B INPUTS

| A1 ——— B4 | A1 ——— B4 | A1 ——— B4 | A1 ——— B4 |

C_{in} CHIP 1 C_{out} | C_{in} CHIP 2 C_{out} | C_{in} CHIP 3 C_{out} | C_{in} CHIP 4 C_{out}

| S1 ——— S4 | S1 ——— S4 | S1 ——— S4 | S1 ——— S4 |

SUM OUTPUTS
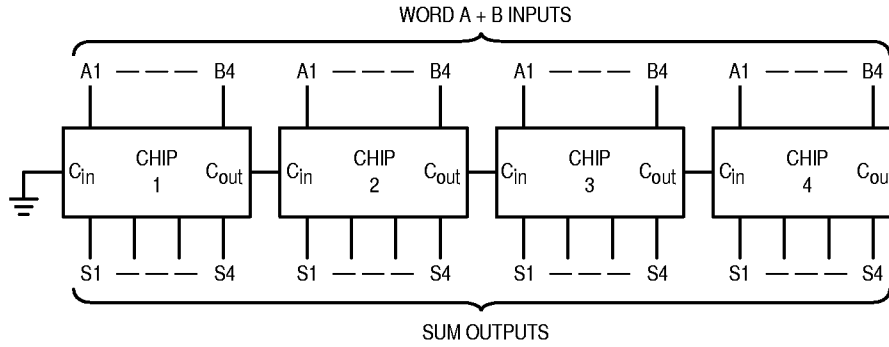
Calculation of 16–bit adder speed:
    t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)
The guaranteed 16–bit adder speed at 10 V, 25°C, C_L = 50 pF is:
    t_p total = 290 + 310 + 300 = 900 ns

Figure 6. Using the MC14008B in a 16–Bit Adder Configuration

L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
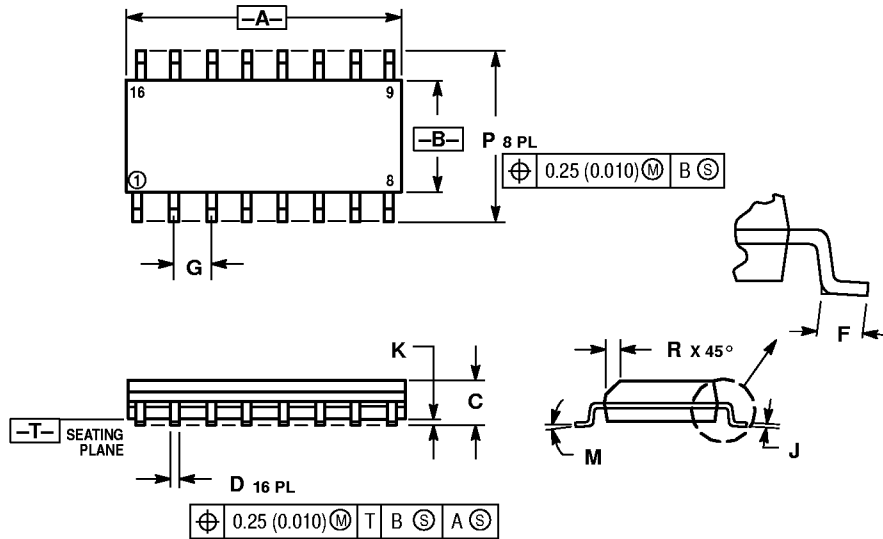
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Ⓜ **MOTOROLA**

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