HD74LS194A

4-bit Bidirectional Universal Shift Register

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Rev.3.00
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The bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs. Operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely;

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

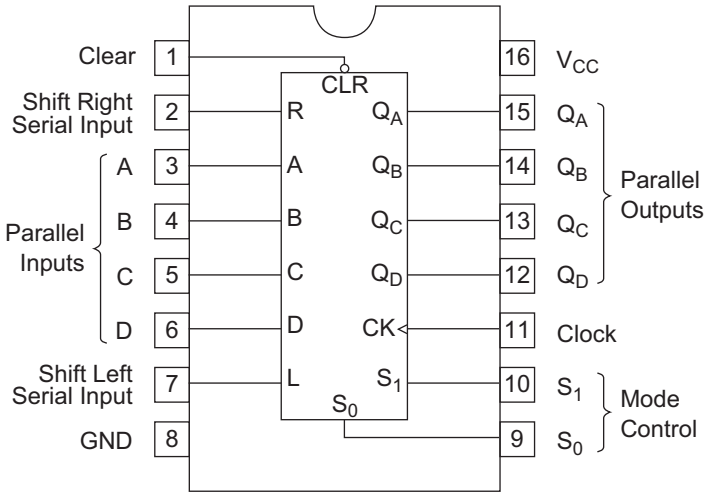
Clocking of the flip-flop is inhibited when both mode control inputs are low.

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS194AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS194AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



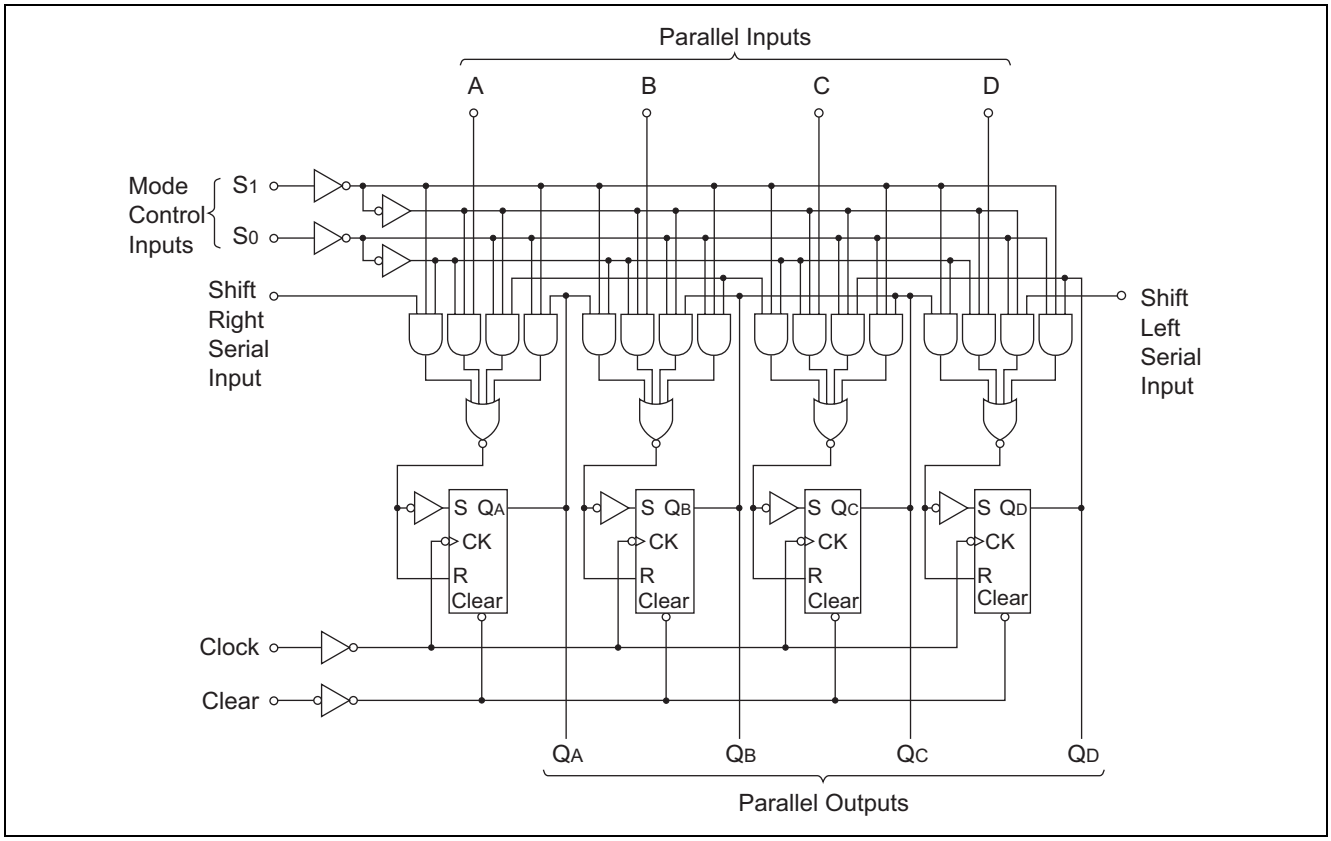
(Top view)

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{Ao}	Q_{Bo}	Q_{Co}	Q_{Do}

Notes: 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a to d; the level of steady-state input at inputs A, B, C, or D, respectively
4. Q_{A0} to Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady-state input conditions were established.
5. Q_{An} to Q_{Dn}; the level of Q_A, Q_B, Q_C, or Q_D, respectively before the most-recent ↑ transition of the clock.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width		$t_{w\,(CK)}$	20	—	—	ns
Clear pulse width		$t_{w\,(CLR)}$	20	—	—	ns
Setup time	Mode Control	t_{su}	30	—	—	ns
	A, B, C, D, R, L		20	—	—	ns
	CLR (inactive state)		25	—	—	ns
Hold time		t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	15	23	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

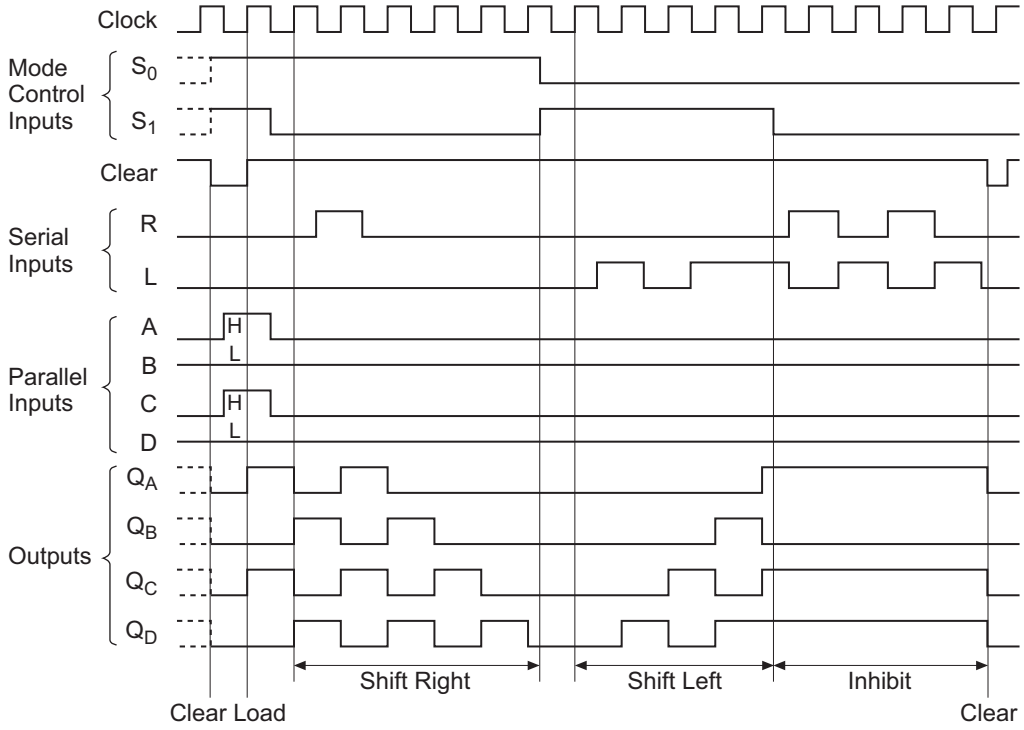
** With all outputs open, inputs A through D grounded, and 4.5 V applied to S_0, S_1, clear and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

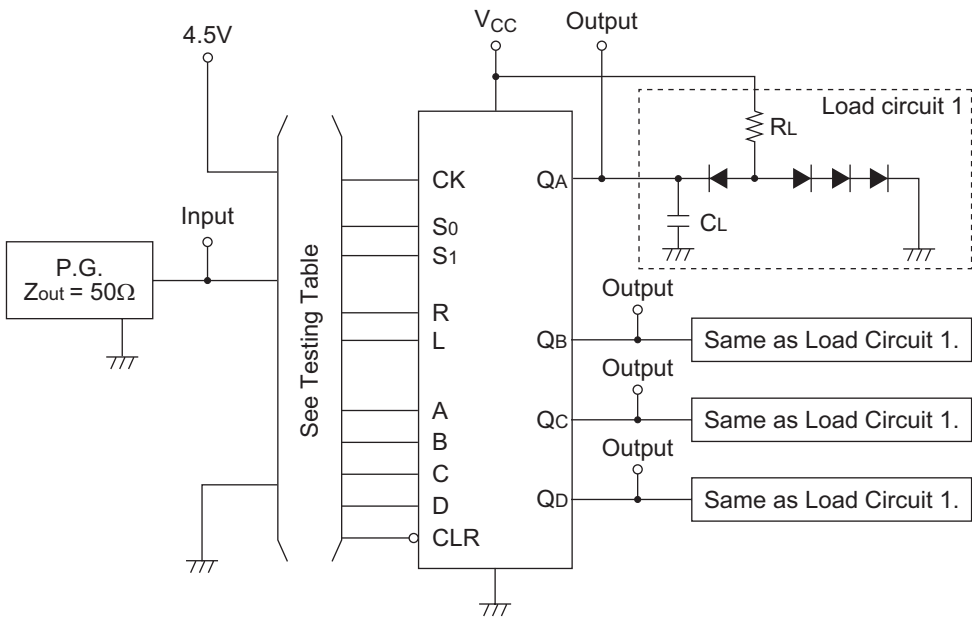
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	36	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PHL}	Clear	Q	—	19	30	ns	
	t_{PLH}	Clock		—	14	22	ns	
	t_{PHL}	Clock		—	17	26	ns	

Count Sequences



Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

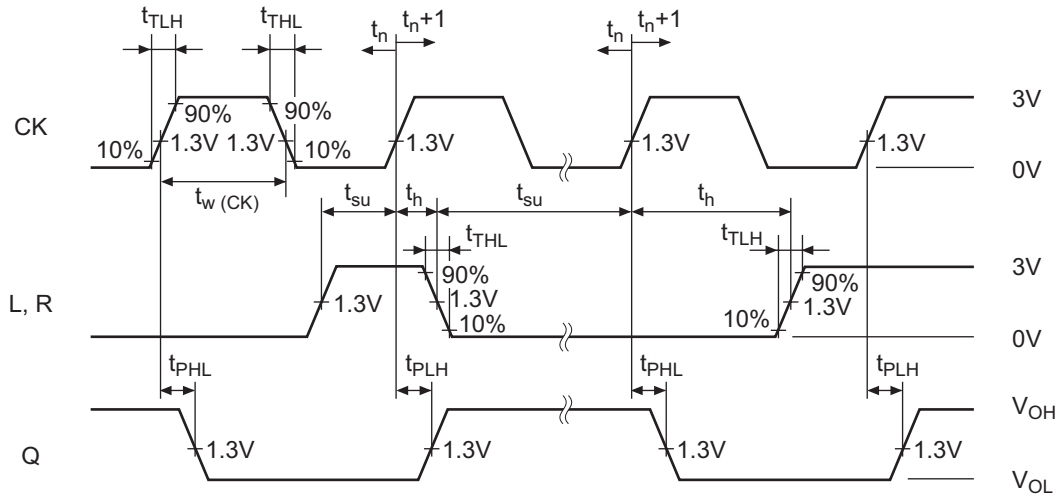
Testing Table

Item	From input to output	Inputs									
		CLR	S_1	S_0	CK	L	R	A	B	C	D
f_{max}	right-shift	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
	left-shift	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	GND	GND
t_{PLH} t_{PHL}	Clear→Q	IN	4.5V	4.5V	IN	GND	GND	4.5V	4.5V	4.5V	4.5V
	Clock→Q	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND
		4.5V	4.5V	GND	IN	IN	4.5V	GND	GND	GND	GND

Item	From input to output	Outputs			
		Q_A	Q_B	Q_C	Q_D
f_{max}	right-shift	OUT	OUT	OUT	OUT
	left-shift	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	Clear→Q	OUT	OUT	OUT	OUT
	Clock→Q	OUT	OUT	OUT	OUT
		OUT	OUT	OUT	OUT

Waveforms 1

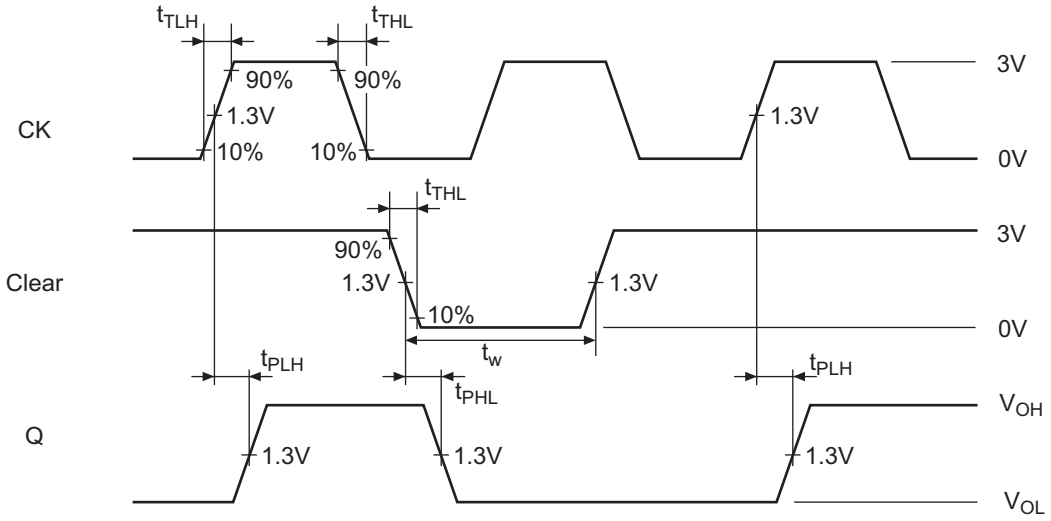
(f_{max}, CK→Q)



Notes: 1. Right-shift is measured with Q_A at t_{n+1}, Q_B at t_{n+2}, Q_C at t_{n+3}, and Q_D at t_{n+4}. Left-shift is measured with Q_A at t_{n+4}, Q_B at t_{n+3}, Q_C at t_{n+2}, and Q_D at t_{n+1}.

Waveforms 2

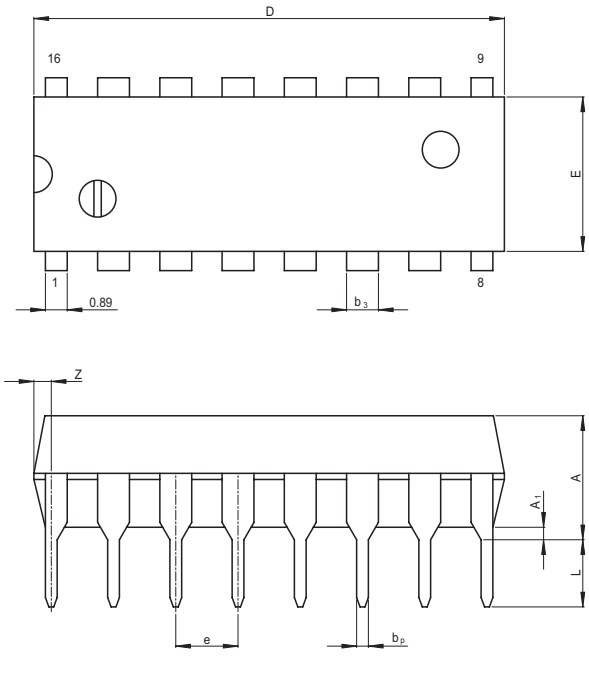
(Clear→Q)



Notes: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns

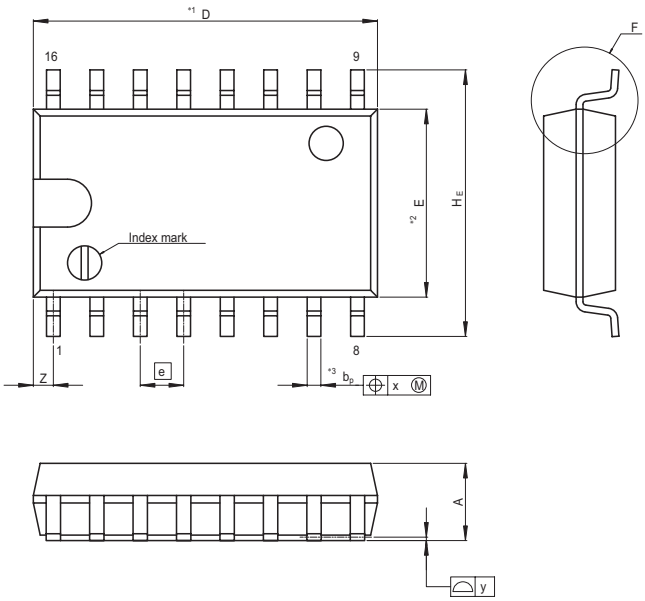
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g

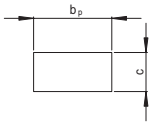


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

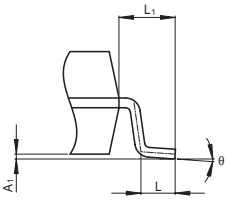
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

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