

HD74LS85

4-bit Magnitude Comparator

REJ03D0421-0200

Rev.2.00

Feb.18.2005

This four bit magnitude comparator performs comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The $A > B$, $A < B$, and $A = B$ outputs of a stage handling less-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the $A \beta B$ input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

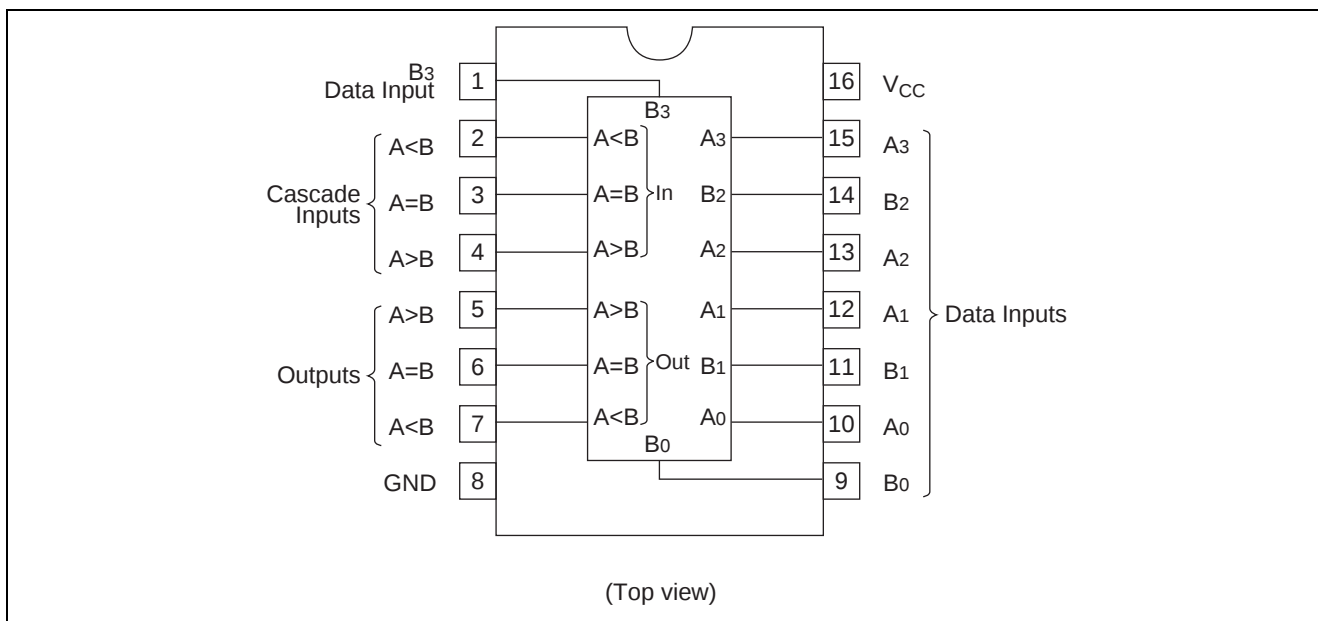
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS85P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS85FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

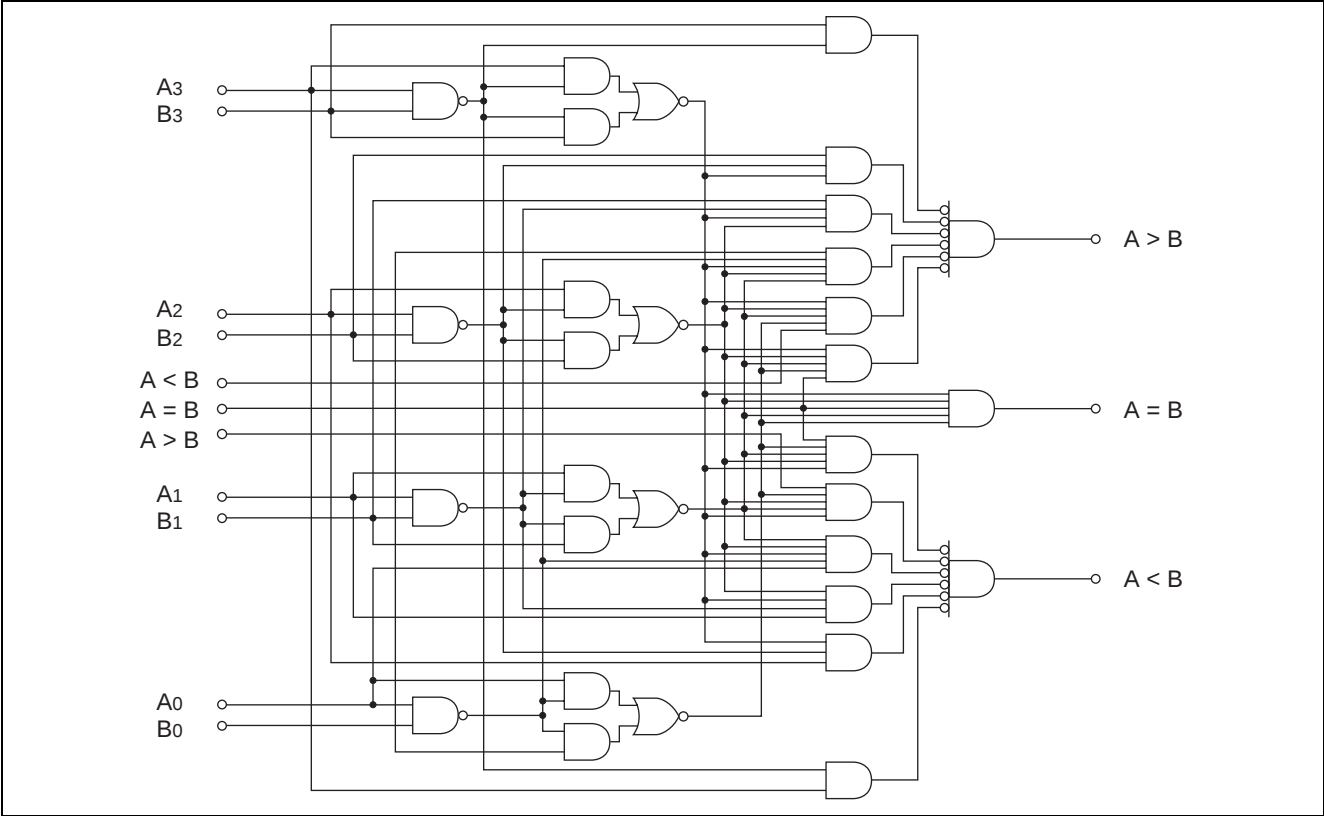


Function Table

Inputs				Cascading Inputs			Outputs		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	A > B	A < B	A = B	A > B	A < B	A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L

H; high level, L; low level, X; irrelevant

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	T _{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	−400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	−20	25	75	°C

Electrical Characteristics

(Ta = −20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	$V_{CC} = 4.75 V$, $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, $I_{OH} = -400 \mu A$
		V_{OL}	—	—	0.4	V	$I_{OL} = 4 mA$ $V_{CC} = 4.75 V$, $V_{IH} = 2 V$, $I_{OL} = 8 mA$ $V_{IL} = 0.8 V$
Input current	A < B, A > B inputs	I_{IH}	—	—	20		$V_{CC} = 5.25 V$, $V_I = 2.7 V$
	Other inputs		—	—	60		
	A < B, A > B inputs	I_{IL}	—	—	−0.4	mA	$V_{CC} = 5.25 V$, $V_I = 0.4 V$
	Other inputs		—	—	−1.2		
	A < B, A > B inputs	I_I	—	—	0.1	mA	$V_{CC} = 5.25 V$, $V_I = 7 V$
	Other inputs		—	—	0.3		
Short-circuit output current		I_{OS}	−20	—	−100	mA	$V_{CC} = 5.25 V$
Supply current**		I_{CC}	—	10.4	20	mA	$V_{CC} = 5.25 V$
Input clamp voltage		V_{IK}	—	—	−1.5	V	$V_{CC} = 4.75 V$, $I_{IN} = -18 mA$

Note: * $V_{CC} = 5 V$, Ta = 25°C** I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

Switching Characteristics

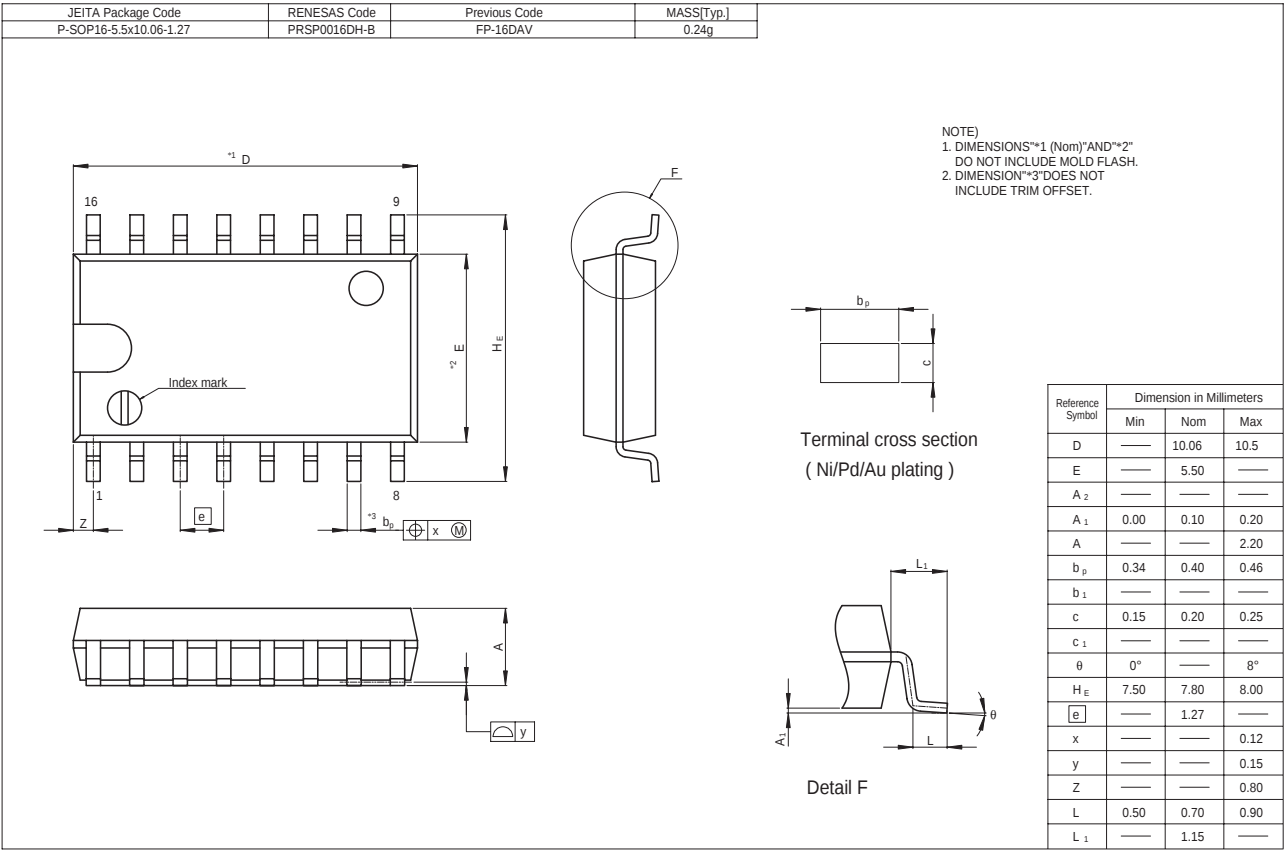
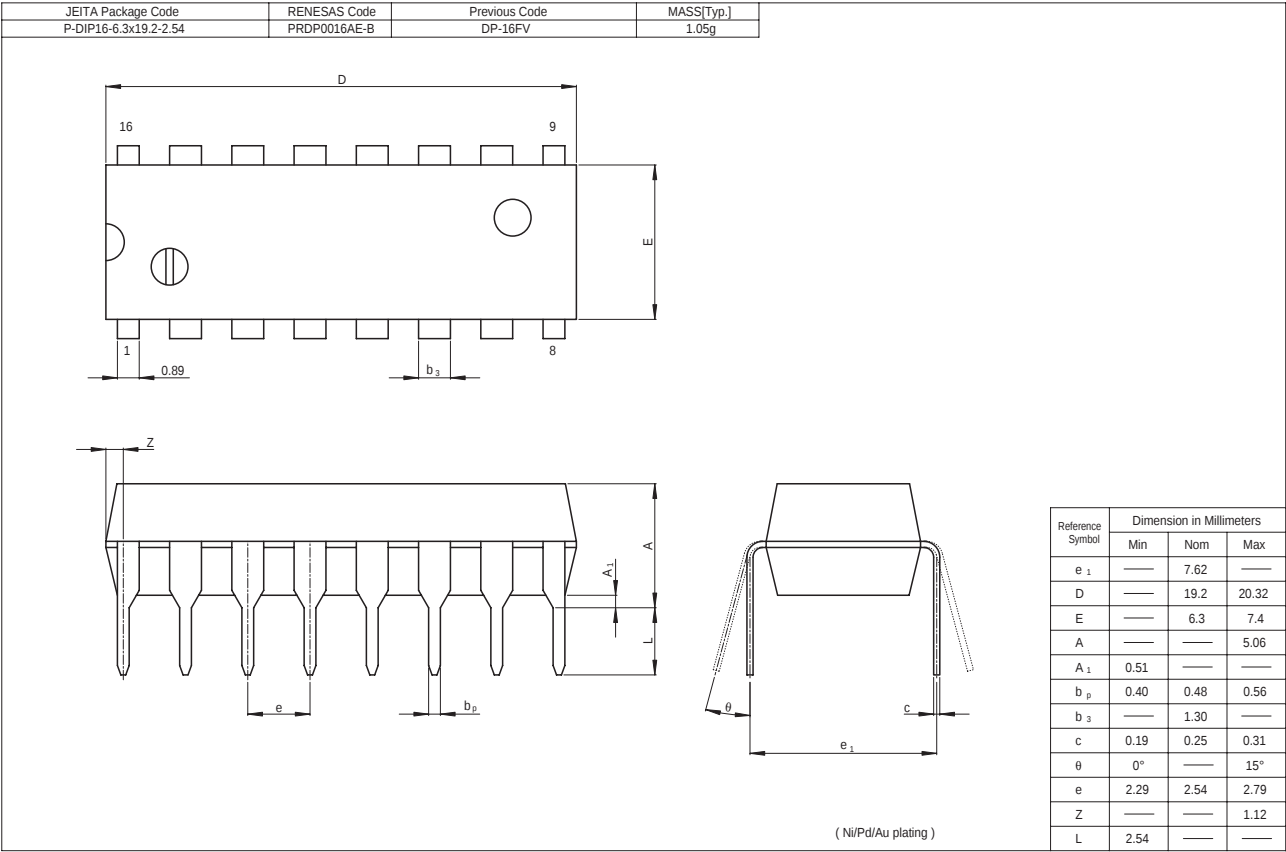
(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	Number of gate levels	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	Any A or B data input	A < B, A > B	1	—	14	—	ns	$C_L = 15 pF$, $R_L = 2 k\Omega$
				2	—	19	—		
				3	—	24	36		
			A = B	4	—	27	45		
	t_{PHL}	Any A or B data input	A < B, A > B	1	—	11	—		
				2	—	15	—		
				3	—	20	30		
			A = B	4	—	23	45		
	t_{PHL}	A < B or A = B	A > B	1	—	14	22		
	t_{PHL}			1	—	11	17		
	t_{PLH}	A = B	A = B	2	—	13	20		
	t_{PHL}			2	—	13	26		
	t_{PLH}	A > B or A = B	A < B	1	—	14	22		
	t_{PHL}			1	—	11	17		

Testing Table

Item	Inputs										Output waveforms			
	A ₃	B ₃	A ₂	B ₂	A ₁	B ₁	A ₀	B ₀	A > B	A = B	A < B	A > B	A = B	A < B
t _{PLH} t _{PHL}	IN	4.5 v	4.5 v	GND	GND	GND	GND	GND	GND	GND	GND	A	—	B
	4.5 v	IN	GND	4.5 v	GND	GND	GND	GND	GND	GND	GND	B	—	A
	GND	GND	IN	4.5 v	4.5 v	GND	GND	GND	GND	GND	GND	A	—	B
	GND	GND	4.5 v	IN	GND	4.5 v	GND	GND	GND	GND	GND	B	—	A
	GND	GND	GND	GND	IN	4.5 v	4.5 v	GND	GND	GND	GND	A	—	B
	GND	GND	GND	GND	4.5 v	IN	GND	4.5 v	GND	GND	GND	B	—	A
	GND	GND	GND	GND	GND	GND	IN	4.5 v	4.5 v	GND	GND	A	—	B
	GND	GND	GND	GND	GND	GND	4.5 v	IN	GND	GND	4.5 v	B	—	A
	GND	GND	GND	GND	GND	GND	IN	4.5 v	GND	4.5 v	GND	—	A	B
	GND	GND	GND	GND	GND	GND	4.5 v	IN	GND	4.5 v	GND	B	A	—
	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	GND	—	—	B
	GND	GND	GND	GND	GND	GND	GND	GND	IN	GND	GND	B	A	B
	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	IN	B	—	—

Package Dimensions



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